102

Supreme Court, U.S.
FILED

2

08-259 AUG 26 2008

No. 08-_____ OFFICE OF THE CLERK

IN THE
Supreme Court of the United States

TRANSLOGIC TECHNOLOGY, INC.,

Petitioner,

v.

HITACHI, LTD., HITACHI AMERICA, LTD.,
AND RENESAS TECHNOLOGY AMERICA, INC.,

Respondents.

**ON PETITION FOR A WRIT OF CERTIORARI
TO THE UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

APPENDICES TO PETITION FOR A WRIT OF CERTIORARI

JEFFREY S. LOVE
JOHN D. VANDENBERG
KLARQUIST SPARKMAN, LLP
121 S.W. SALMON STREET
SUITE 1600
PORTLAND, OREGON 97204
(503) 226-7391

ROBERT A. LONG
COUNSEL OF RECORD
E. EDWARD BRUCE
RICHARD L. RAINEY
BRIAN G. BIELUCH
GREGORY M. LIPPER
MICHAEL N. KENNEDY
JOSHUA B. SIMMONS
COVINGTON & BURLING LLP
1201 PENNSYLVANIA AVENUE, NW
WASHINGTON, D.C. 20004
(202) 662-6000

Counsel for Petitioner

AUGUST 2008

TABLE OF CONTENTS

Page

Appendix A (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Nos. 2005-1387, 2006-1333 (Fed. Cir. Oct. 12, 2007)) (vacating judgment and remanding for dismissal) 1a

Appendix B (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Apr. 6, 2006)) (opinion and order, *inter alia*, denying defendants' motion for a new trial)..... 6a

Appendix C (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Dec. 13, 2005)) (opinion on defendants' motion for judgment as a matter of law and reconsideration)..... 21a

Appendix D (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Dec. 13, 2005)) (final judgment that the '666 patent is infringed by defendants and is not invalid)..... 36a

Appendix E (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. May 6, 2005)) (jury verdict finding induced infringement and awarding Translogic $86.5 million in damages) 40a

Appendix F (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Feb. 22, 2005)) (adopting Special Master's recommendation that Translogic is entitled to summary judgment of infringement) 42a

Appendix G (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Dec. 7, 2004)) (report and recommendation of Special Master regarding infringement) 48a

Appendix H (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Civ. No. 99-407-PA (D. Or. Feb. 9, 2004)) (denying defendants' motions for a new trial and judgment as a matter of law). 107a

Appendix I (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.* Civ. No. 99-407-PA (D. Or. Oct. 28, 2003)) (jury verdict finding '666 patent not invalid as either anticipated or obvious). 126a

Appendix J (*In re Translogic Technology, Inc.*, No. 06-1192 (Fed. Cir. Jan. 24, 2008)) (order denying petition for panel rehearing and rehearing *en banc* in companion case) 130a

Appendix K (*In re Translogic Technology, Inc.*, 504 F.3d 1249 (Fed. Cir. 2007)) (opinion affirming findings of Board of Patent Appeals and Interferences in companion case) 133a

Appendix L (Ex parte *Translogic Technology, Inc.*, Appeal No. 2005-1050 (B.P.A.I. Oct. 26, 2005)) (opinion denying rehearing in companion case) 161a

Appendix M (Ex parte *Translogic Technology, Inc.*, Appeal No. 2005-1050 (B.P.A.I. July 14, 2005)) (order of Board of Patent Appeals and Interferences in companion case)..... 182a

Appendix N (*Translogic Technology, Inc. v. Hitachi, Ltd., et al.*, Nos. 2005-1387, 2006-1333 (Fed. Cir. May 29, 2008)) (order denying panel rehearing and rehearing *en banc*) 266a

APPENDIX A

NOTE: This disposition is nonprecedential.

United States Court of Appeals

for the Federal Circuit

2005-1387, 2006-1333

TRANSLOGIC TECHNOLOGY, INC.,

Plaintiff-Appellee,

v.

HITACHI, LTD., HITACHI AMERICA, LTD., and RENESAS TECHNOLOGY AMERICA, INC.,

Defendants-Appellants.

Jeffrey S. Love, Klarquist Sparkman, LLP, of Portland, Oregon, argued for plaintiff-appellee. With him on the brief were Jared S. Goff and John D. Vandenberg. Of counsel was Kevin M. Hayes.

James G. Gilliland, Jr., Townsend and Townsend and Crew LLP, of Palo Alto, California, argued for defendants-appellants. With him on the brief were Madison C. Jellins and D. Stuart Bartow.

Of counsel on the brief were David Axelrod, Schwabe, Williamson & Wyatt, P.C., of Portland, Oregon, and Nathan Lane III, Squire, Sanders & Dempsey L.L.P., of San Francisco, California, and David S. Elkins of Palo Alto, California.

Appealed from: United States District Court for the District of Oregon

Senior Judge Owen M. Panner

NOTE: This disposition is nonprecedential.

United States Court of Appeals

for the Federal Circuit

2005-1387, 2006-1333

TRANSLOGIC TECHNOLOGY, INC.,

Plaintiff-Appellee,

v.

HITACHI, LTD., HITACHI AMERICA, LTD., and RENESAS TECHNOLOGY AMERICA, INC.,

Defendants-Appellants.

DECIDED: October 12, 2007

Before MAYER, RADER, and PROST, Circuit Judges.

RADER, Circuit Judge.

The United States District Court for the District of Oregon entered judgment against Hitachi, Ltd., Hitachi America, Ltd., and Renesas Technology America, Inc. ("Hitachi") for infringement of U.S.

Patent No. 5,162,666 ("the '666 patent") owned by Translogic Technology, Inc. ("Translogic"). Translogic Tech., Inc. v. Hitachi, Ltd., Hitachi Am., Ltd., and Renesas Tech. Am., Inc., Civ. No. 99-407-PA, (D. Or. May 12, 2005) ("Opinion"); Translogic Tech., Inc. v. Hitachi, Ltd., Hitachi Am., Ltd., and Renesas Tech. Am., Inc., Civil Action No.: 3-99-00407-PA (D. Or. December 13, 2005) ("Final Judgment"). The judgment imposed monetary damages and a permanent injunction. Id. The '666 patent describes a multiplexer circuit "formed of two-to-one transmission gate multiplexer ("TGM") circuits connected in series." '666 Patent Abstract.

In a parallel case before the same panel of this court, Translogic appealed the decision of the United States Patent and Trademark Office's Board of Patent Appeals and Interferences ("Board") upholding a patent examiner's rejection, in reexamination, of the '666 patent. Ex parte Translogic Tech., Inc., Appeal No. 2005-1050, Board of Patent Appeals and Interferences (July 14, 2005) (Request for Rehearing denied on October 26, 2005). The Board held the claims of the '666 patent obvious based on prior art references disclosing series multiplexer circuits in view of a 1985 textbook disclosing TGM circuits. Id. This court, in a precedential opinion, affirmed the Board's decision that the claims of the '666 patent are obvious under 35 U.S.C. § 103(a). In re Translogic Tech., Inc., ---- F.3d ---- (Fed. Cir. 2007). In light of this court's decision in In re Translogic Tech., Inc., this court vacates the district court's decision and remands this case to the district court for dismissal.

VACATED and REMANDED

COSTS

Each party shall bear its own costs.

APPENDIX B

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed APR 6, 2006]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Civ. No. 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., and RENESAS TECHNOLOGY AMERICA, INC.,	)	OPINION AND ORDER
Defendants.	)	

JEFFREY STEWART LOVE
JARED S. GOFF
JOHN D. VANDENBERG
Klarquist Sparkman, LLP
One World Trade Center
121 S.W. Salmon Street
Suite 1600
Portland, OR 97204-2988

Attorneys for Plaintiff

DAVID AXELROD
Schwabe Williamson & Wyatt, P.C.
Pacwest Center, Suite 1600-1800
1211 S.W. Fifth Avenue
Portland, OR 97204-3795

Nathan Lane III
David S. Elkins
Jose L. Martin
Squire, Sanders & Dempsey L.L.P.
One Maritime Plaza, Third Floor
San Francisco, California 94111-3492

Attorneys for Defendants

PANNER, J.

Plaintiff Translogic Technology, Inc. brings this action for infringement of U.S. Patent No. 5,162,666 (the '666 Patent), for multiplexers used in microprocessors. The defendants are Hitachi Ltd., Hitachi America, Ltd., and Renesas Technology America, Inc.

In the first trial, the jury found that claims 16 and 17 of the '666 Patent were not anticipated, and this court found that the claims were not obvious. In the second trial, the jury found that defendants had infringed claims 16 and 17; that Hitachi, Ltd. had induced infringement; and that plaintiff was entitled to $86.5 million in damages.

Defendants now move a new trial and to stay enforcement of the judgment pending appeal. I deny the motions.

I. Defendants' Motion for a New Trial

Plaintiff contends that defendants waived the errors now cited in defendants' motion for a new trial. I conclude, however, that defendants adequately raised the alleged errors during the trial.

A. Standards

The court may grant a motion for a new trial if the jury's verdict is contrary to the clear weight of the evidence, if the verdict is based on false evidence, or if there would otherwise be a miscarriage of justice. See Roy v. Volkswagen of America, Inc., 896 F.2d 1174, 1176 (9th Cir.), as amended by 920 F.2d 618 (9th Cir. 1990). "While the trial court may weigh the evidence and credibility of the witnesses, the court is not justified in granting a new trial 'merely because it might have come to a different result from that reached by the jury.'" Id. (quoting Wilhelm v. Associated Container Transp. (Australia) Ltd., 648 F.2d 1197, 1198 (9th Cir. 1981)). The district court has discretion in deciding whether to grant a new trial. Unocal Corp. v. United States, 222 F.3d 528, 534 (9th Cir. 2000).

B. Discussion

1. Admission of Licensing Negotiations

Defendants contend that this court improperly allowed plaintiff to present evidence of settlement negotiations between the parties, violating Federal Rule of Evidence 408. Plaintiff presented evidence that it had offered to license its patent to defendants for three years for $40 million, plus defendants'

agreement to help plaintiff market its technology. Defendants contend that the jury must have relied on this evidence in calculating damages.

Plaintiff argues that the evidence was properly admitted because the parties were engaged in license negotiations, not settlement discussions. Plaintiff states that the discussions were forward-looking.

This has been an on-going dispute in this litigation. I ruled as follows after the first trial on validity:

> Defendants object to admission of the inventor's notes on a 1997 meeting with defendants' representatives, contending that these notes are inadmissible under Federal Rule of Evidence 408. Rule 408 generally excludes "[e]vidence of conduct or statements made in compromise negotiations."
>
> Defendants cite an August 1997 letter to defendants from Marvin Bush, who was then plaintiff's president, stating that one purpose of the February 1997 meeting was to "inform Hitachi" of alleged infringement of plaintiff's '666 Patent.
>
> I agree with plaintiff that the inventor's notes of the meeting with defendants were admissible because plaintiff had not yet made a claim of infringement at that time. See Deere & Co. v. International Harvester Co., 710 F.2d 1551, 1557 (Fed. Cir. 1983) (exclusion of evidence under Rule 408 limited to "actual

> disputes over existing claims"; party's offer to license patent admissible because no accompanying charge of infringement). Cf. Red Wing Shoe Co. v. Hockerson-Halberstadt, Inc., 148 F.3d 1355, 1361 (Fed. Cir. 1998).
>
> Defendants also argue that the inventor's notes were inadmissible hearsay. However, the inventor took the notes in the regular course of business, and statements by defendants' representatives are admissible as the admissions by a party opponent. Even if the notes themselves were not admissible, admission of the notes was harmless because the inventor was entitled to testify about statements he had heard.

I adhere to my prior rulings and conclude that evidence of the parties' license negotiations was admissible.

2. Excessive Damages

Defendants contend that the award of damages was excessive. When a party seeks a new trial on the amount of damages, the trial court "determines whether the jury's verdict is against the clear or great weight of the evidence." Unisplay v. American Elec. Sign Co., 69 F.3d 512, 517 (Fed. Cir. 1995) (quotation marks and citation omitted).

Defendants contend that the award is not supported by substantial evidence; is grossly excessive in light of defendants' profits and sales, and the amount plaintiff obtained from its only license; and is based only on speculation and guesswork.

Plaintiff responds that the inventor Tran's testimony on the amount of a reasonable royalty is sufficient to support the amount of damages. Plaintiff contends that Tran is qualified to testify on the amount of a reasonable royalty.

Defendants contend that Tran had no evidence to support his royalty figures, such as whether a reasonable "seat license" for each engineer would reasonably be valued at $70,000, or whether a company the size of Hitachi, Ltd., would require 200 engineers to be licensed.

Plaintiff also argues that it presented other evidence supports the jury's damages award, such as evidence that redesign costs would have been in the hundreds of millions of dollars, and that the infringing microprocessors were "flagship products" worth a great deal to defendants.

I have carefully examined all of the evidence regarding damages. I conclude that the jury's award of damages was not against the great weight of the evidence.

3. Lost Profits

Defendants contend that this court improperly allowed plaintiff to assert claims for lost profits, damages suffered because defendants contested validity, and damages for Dr. Yano's publication of technical papers.

Plaintiff responds that it did not seek lost profits. Lost profits are not mentioned in the verdict form, and plaintiff states that it did not argue for lost profits. Plaintiff states that it had a valid reason to

introduce evidence that defendants contested the patent: to show that the Intel would have paid more for its license with plaintiff but for Intel's knowledge that defendants were contesting the validity of plaintiff's patent.

I agree with plaintiff that it did not seek lost profits, and that it was not improper for plaintiff to present evidence that defendants are challenging the validity of the patent.

4. Exclusion of Reexamination Proceedings

Defendants contend that this court erred in excluding evidence of the reexamination proceedings. Defendants contend that plaintiff was able to imply at trial that defendants had willfully infringed the patent (despite this court's ruling to the contrary) because defendants could not cite the reexamination proceedings as evidence that defendants reasonably believed the patent was invalid.

This has been another ongoing dispute. This court has excluded evidence of the reexamination proceedings to prevent jury confusion and undue delay. I adhere to my prior rulings. Even if the rulings were wrong, excluding evidence of the reexamination proceedings does not justify a new trial.

5. Exclusion of Intel Witness O'Hara

Defendants contend that this court erred in excluding testimony of Randy O'Hara, who was employed by Intel during Intel's licensing

negotiations with plaintiff. Defendants argue that O'Hara would have testified that (1) the dispute between plaintiff and defendants had no effect on Intel's licensing negotiations with plaintiff, and (2) Intel did not know of any use of the subject matter licensed from plaintiff. When asked whether the dispute between plaintiff and defendants affected Intel's negotiations with plaintiff, O'Hara, who helped negotiate for Intel, stated, "I don't think so." Defendants contend that this answer meant "No," rather than showing that O'Hara had no personal knowledge of the issue.

I agree with plaintiff that O'Hara's excluded testimony indicated that he had no personal knowledge of the subjects raised. Even if it was error to exclude this testimony, such an error would not justify a new trial.

6. Disparate Treatment of Witnesses and Counsel

Defendants contend that this court favored plaintiff's witnesses and counsel over defendants' witnesses and counsel. Defendants argue that this court precluded them from presenting testimony rebutting evidence on the reasonableness of plaintiff's 1997 royalty offer, while allowing Tran to testify on matters outside his witness statement. Defendants complain that this court limited their witnesses' testimony based on witness statements, which implied to the jury that defendants were acting improperly.

Defendants have not shown that I improperly favored plaintiff during the trial. Defendants'

perception of unfairness may be related to their lack of success at trial.

7. Failure to Give Requested Jury Instructions

Defendants contend that this court erred by failing to give four jury instructions requested by defendants.

a. Standards

Jury instructions must fairly and sufficiently address the issues, state the law accurately, and must not mislead the jury. Duran v. City of Maywood, 221 F.3d 1127, 1130 (9th Cir. 2000). In evaluating jury instructions, the court should consider the instructions as a whole. Guebara v. Allstate Ins. Co., 237 F.3d 987, 992 (9th Cir. 2001).

b. Instruction No. 4: Infringement Not Willful

Defendants' requested instruction no. 4 stated that the court had determined that any infringement by defendants was not willful because defendants had a reasonable belief that the patent was invalid, and that willfulness was not an issue for trial. Defendants contend that the failure to give this instruction left the jury with the impression that defendants had no reason to assert invalidity, and that defendants unreasonably rejected the license offered by plaintiff.

Failure to give the instruction was not error. I did not want to confuse the jury by raising the issue

of willfulness. The proposed instruction itself says willfulness is not an issue.

c. Instruction No. 28: Infringing Circuitry is Basis for Consumer Demand

Defendants sought an instruction that the infringing circuitry must be the basis for consumer demand to justify plaintiff's recovery of damages for the entire market value of the microprocessor. I rejected this instruction as a comment on the evidence.

The jury was sufficiently instructed on damages. This court correctly instructed the jury that one royalty factor is the portion of profit arising from the patented invention, as opposed to profit arising from features unrelated to the patented invention, such as the manufacturing process, business risks, or significant features or improvements added by the infringer. This sufficiently covers the issue.

d. Instruction No. 23: Parties Deemed to Know Nature and Extent of Infringement

Defendants contend that this court should have given their proposed instruction that at the time of the hypothetical licensing negotiations, defendants should be presumed to know "the nature and extent of Hitachi's use of the invention and the level of sales and profits that Hitachi would make using the invention."

I instructed the jury to consider "[t]he extent to which the accused infringer has made use of the invention." This instruction adequately covers the issue.

e. Instruction No. 27: Non-Infringing Alternatives

Defendants contend that this court erred in failing to give their proposed instruction on whether non-infringing substitutes were available at the time of the hypothetical negotiations. I did instruct the jury to consider "[t]he utility and advantages of the patented invention over the old modes or devices, if any, that had been used for achieving similar results." The jury instructions as given sufficiently covered the issue.

II. Defendants' Motion to Stay Judgment Pending Appeal

Defendants move under Federal Rule of Civil Procedure 62(d) for a stay of enforcement of the judgment. Defendants' motion includes three alternate requests:

(1) to relieve defendants of any requirement to post security for the judgment pending appeal;

(2) if the first alternate is denied, to condition denial on plaintiff's posting an undertaking that assures defendants that plaintiff can pay the costs of posting security if costs are awarded to defendants on appeal; and

(3) if both alternates (1) and (2) are denied, to stay enforcement while defendants file an appeal from

that denial with the Federal Circuit and, if that appeal is denied, to stay for the time needed to obtain and deliver a letter of credit securing payment of the judgment. and interest.

Plaintiff opposes the motion.

A. Background

On December 13, 2005, this court entered a judgment against defendants for $86.5 million in damages, and more than $18 million in prejudgment interest. Defendants state that posting security would cost them $1.5 million if the appeal takes 2.5 years.

In lieu of posting security, defendants offered to provide plaintiff with a written promise of prompt payment after all appeals expire. Plaintiff rejected this offer, stating that it would accept a payment of $250,000 "to offset its added risks and expenses," along with an adequate assurance of prompt, full payment of judgment. Negotiations were not successful and defendants filed this motion.

B. Discussion

Federal Rule of Civil Procedure 62(d) provides:

> When an appeal is taken the appellant by giving a supersedeas bond may obtain a stay subject to the exceptions contained in subdivision (a) of this rule. The bond may be given at or after the time of filing the notice of appeal or of procuring the order allowing the appeal, as the case may be. The stay is

> effective when the supersedeas bond is approved by the court.

An appellant may also obtain a stay by providing alternative security to the judgment creditor, subject to the court's approval. See International Telemeter Corp. v. Hamlin Int'l Corp., 754 F.2d 1492, 1495 (9th Cir. 1985). Rule 62(d)

> is largely a procedural mechanism to preserve the status quo of the parties during the pendency of the appeal; its primary purpose is to protect the prevailing plaintiff from the risk of a later uncollectible judgment and compensate the plaintiff for delay in the entry of final judgment. Bass v. First Pac. Networks. Inc., 219 F.3d 1052, 1055 (9th Cir. 2000) (citations omitted). In that respect, the court has wide discretion in setting the appropriate bond or alternative security. The court is to be guided by general equitable principles, with the overarching purpose being to safeguard the judgment creditors as completely as possible without irreparably injuring the judgment debtors. Texaco, Inc. v. Pennzoil Co., 784 F.2d 1133, 1155 (2d Cir. 1986) [rev'd, 481 U.S. 1 (1987)].

LPP Mortg. Ltd. v. Gardner, Civ. No. 02-1331-AS, 2005 WL 2078339, *1 (D. Or. Aug. 16, 2005).

Here, defendants cite a Seventh Circuit opinion, Dillon v. City of Chicago, 866 F.2d 902, 904-05 (7th Cir. 1988), for five factors courts should consider in deciding whether to require security:

(1) the complexity of the collections process;

(2) the time required to obtain a judgment after it is affirmed on appeal;

(3) the degree of confidence the court has in the availability of funds to pay the judgment;

(4) whether the defendant's ability to pay the judgment is so plain that the cost of a bond would be a waste of money; and

(5) whether the defendant is in such a precarious financial situation that the requirement to post a bond would place other creditors in an insecure position.

(Plaintiff notes that the Ninth Circuit has not adopted these factors.) Defendants' main argument is that their ability to pay the judgment should be beyond dispute. Defendants state that Hitachi Ltd. has more than $95 billion in assets, including $7 billion in cash and cash equivalents, revenues of $90 billion per year, and stockholders' equity of about $20 billion.

Plaintiff responds that recent corporate collapses have shown that size is no guarantee of solvency. Plaintiff also states that defendants have fought every step of this litigation, so it expects defendants to fight enforcement of the judgment as well. Plaintiff contends that a "bare 'promise'" from defendants is insufficient given the size of the judgment.

I see no reason to depart from the usual practice of requiring a bond-pending appeal. Defendants' size does not justify departing from this practice.

Regarding the second alternate motion, I agree with plaintiff that neither plaintiff nor non-parties such as Tran should be required to post a bond to cover the costs of defendants' supersedeas bond. Defendants cite no precedent for requiring that an appellee post for a bond.

In defendants' third alternate motion, they request that this court stay the bond requirement while they appeal to the Federal Circuit. I deny the request. Defendants are free to seek a stay with the appellate court.

CONCLUSION

Defendants' motions for a new trial (#846) and to stay the judgment pending appeal (#843) are denied.

DATED this 5 day of April, 2006.

/s/ Owen M. Panner

OWEN M. PANNER
U.S. DISTRICT JUDGE

APPENDIX C

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed DEC 13, 2005]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Civ. No. 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	OPINION
Defendants.	)	

JEFFREY STEWART LOVE
KEVIN M. HAYES
Klarquist Sparkman, LLP
One World Trade Center
121 SW Salmon Street
Suite 1600
Portland, OR 97204-2988

Attorneys for Plaintiff

DAVID AXELROD
Schwabe Williamson & Wyatt, P.C.
Pacwest Center, Suite 1600-1800
1211 S.W. Fifth Avenue
Portland, OR 97204-3795
Nathan Lane III
David S. Elkins
Jose L. Martin
Squire, Sanders & Dempsey L.L.P.
One Maritime Plaza, Third Floor
San Francisco, California 94111-3492

Attorneys for Defendants

PANNER, J.

Plaintiff Translogic Technology, Inc. brings this action for infringement of U.S. Patent No. 5,162,666 (the '666 Patent), for transmission gate series multiplexers used in microprocessors. The defendants are Hitachi Ltd., Hitachi America, Ltd., and Renesas Technology America, Inc.

In the first trial, the jury found that claims 16 and 17 of the '666 Patent were not anticipated, and this court found that the claims were not obvious. In the second trial, the jury found that defendants had infringed claims 16 and 17; that Hitachi, Ltd. had induced infringement; and that plaintiff was entitled to damages.

Defendants move for judgment as a matter of law on plaintiff's inducement claims as to third-parties; to reconsider the denial of defendants' previous motion for judgment as a matter of law on

anticipation; and to partially reconsider claim construction. I deny defendants' motions.

DISCUSSION

In an appeal from this court's judgment, the Federal Circuit will apply its own law to substantive patent issues. Ninth Circuit law governs the procedural standards for defendants' post-trial motions. Shockley v. Arcan, Inc., 248 F.3d 1349, 1358 (Fed. Cir. 2001).

I. Judgment as a Matter of Law on Third-Party Inducement Claims

Defendants move for judgment as a matter of law on plaintiff's claims that Hitachi, Ltd., induced Sega Enterprises Ltd. of Japan (Sega Japan) and Casio Computer Co., Ltd. of Japan (Casio Japan) to infringe plaintiff's patent. Plaintiff alleges that Sega Japan's Dreamcast product and Casio Japan's Classpad 300 calculator were imported into the United States and contain microprocessors made by Hitachi, Ltd. that include infringing circuits, and that Hitachi, Ltd. encouraged Sega Japan and Casio Japan to import products containing infringing circuits.

A. Standards for Judgment as a Matter of Law

In analyzing a motion for judgment as a matter of law, the court must view the evidence in the light most favorable to the nonmoving party, and draw all reasonable inferences in favor of that party. Horphag Research Ltd. v. Pellegrini, 337 F.3d 1036, 1040 (9th Cir. 2003), cert. denied, 540 U.S. 1111

(2004). To grant a motion for judgment as a matter of law, the court must find that there is "no legally sufficient evidentiary basis for a reasonable jury to find" in favor of the nonmoving party. Fed. R. Civ. P. 50 (a) (1) .

"Judgment as a matter of law is proper when the evidence permits only one reasonable conclusion and the conclusion is contrary to that reached by the jury." Ostad v. Oregon Health Sciences Univ., 327 F.3d 876, 881 (9th Cir. 2003). The court may not substitute its view of the evidence for that of the jury. See Costa v. Desert Palace, Inc., 299 F.3d 838, 859 (9th Cir. 2002) (en banc), aff'd, 539 U.S. 90 (2003). The court may not determine credibility or weigh evidence. Id.

B. Discussion

Here, the jury was instructed that to establish inducement, plaintiff was required to prove that (1) Hitachi, Ltd., encouraged or instructed another person to perform an infringing act; (2) Hitachi, Ltd., knew of the '666 Patent; (3) Hitachi, Ltd., knew or should have known that its encouragement or instructions would likely result in the other person importing into or selling in the United States the end-product containing a microprocessor with infringing circuits; and (4) the other person infringed the '666 patent.

A patentee may use circumstantial evidence to prove intent to induce infringement, and the fact-finder may infer intent from the evidence. See MEMC Elec. Materials, Inc. v. Mitsubishi Materials Silicon Corp., 420 F.3d 1369, 1380-81 (Fed. Cir.

2005) (citations omitted) (reversing summary judgment for the alleged inducer on an inducement claim supported by circumstantial evidence). Intent is a factual determination "particularly within the province of the trier of fact." Allen Organ Co. v. Kimball Int'l, Inc., 839 F.2d 1556, 1567 (Fed. Cir. 1988) (proof of inequitable conduct).

Here, the evidence was sufficient for a jury to find that Hitachi, Ltd. induced Casio Japan and Sega Japan to infringe the '666 Patent. Although evidence of Hitachi, Ltd.'s intent was largely circumstantial, the jury could infer intent to induce infringement from the evidence plaintiff presented regarding Hitachi Ltd.'s conduct, including Hitachi, Ltd.'s marketing plans and sales meetings with Casio Japan and Sega Japan.

Regarding Sega Japan, the parties stipulated that Hitachi, Ltd. sold more than 10 million units of SH7091, SH7091R, and SH7091T microprocessors to Sega Japan, for $288 million; that Hitachi, Ltd. knew that Sega Japan was using the microprocessors in its Dreamcast product; that employees of Renesas Technology America, Inc. met with Sega of America, Inc. employees to discuss the use of SH-4 microprocessors and the Dreamcast product; that Hitachi, Ltd. knew that Dreamcast products containing the SH7091, SH7091R, and SH7091T microprocessors were imported and sold in the United States; and that about 15% of the SH7091, SH7091R, and SH7091T microprocessors sold by Hitachi, Ltd. to Sega Japan in Japan for $49 million were later sold as part of Dreamcast products in the United States. A reasonable jury could infer from the evidence that Hitachi, Ltd. sold infringing

microprocessors to Sega Japan and encouraged Sega Japan to use the infringing microprocessors in Dreamcast products that Hitachi, Ltd. knew would be imported into the United States, and that Sega Japan did import the Dreamcast products into the United States.

The evidence was also sufficient for the jury to find Hitachi, Ltd. liable for inducing infringement as to Casio Japan.

Because I deny defendants' motion for judgment as a matter of law on the merits, I need not address plaintiff's contention that defendants failed to raise these issues at trial.

II. Motion to Reconsider Denial of Judgment as a Matter of Law on Anticipation

Defendants seek reconsideration of this court's order denying judgment as a matter of law on defendants' anticipation defense. At the validity trial, the jury found that claims 16 and 17 of the '666 Patent were not anticipated by prior art. I denied defendants' motion for judgment as a matter of law on anticipation.

Defendants now contend that I should adopt the most recent claim construction of the Board of Patent Appeals and Interferences (the Board) regarding the significance of intermediate outputs that are connected to circuits outside of the multiplexer circuit. Defendants argue that if the Board's claim construction is adopted, then this court must hold that three prior art references anticipate claim 16 of the '666 Patent: the Oklobzija article,

Goto Japanese patent JP '531, and Goto Japanese patent JP '529.[1]

A. The Board's Rulings Do Not Require Reconsideration

Defendants argue that the Board's opinion and claim construction "are part of the file history of the '666 patent, and so must be considered as part of the claim construction process. This portion of the file history was not available to the Special Master and the Court at the time the original claim construction order was entered."

Plaintiff filed this action in March 1999. Because of the reexamination proceedings that began in July 1999, in September 1999, this court granted defendants' motion to stay.

In December 2002, the court lifted the stay of litigation because the reexamination proceedings appeared likely to continue for years. This court determined that plaintiff deserved its day in court, despite the possibility that the reexamination proceedings might some day produce rulings that were inconsistent with this court's rulings. The Special Master reviewed the reexamination file up to that time in writing his report on claim construction. This court held the trial on validity in October 2003.

Meanwhile, reexamination proceedings proceeded at a somewhat slower pace. Cf. 35 U.S.C. §

---

[1] The parties are familiar with the full citations for these items of prior art.

305 (reexamination proceedings must be conducted with "special dispatch"). The PTO granted the request for reexamination in July 1999. Six years and five reexaminations later, the Board issued the claim construction on which defendants now rely.

If a district court was obliged to alter its claim construction to conform to a later claim construction issued by the Board, then there would be no reason to proceed with litigation while reexamination proceedings were pending. District courts are not, however, bound by the Board's rulings, and district courts are not required to stay litigation under these circumstances. See Vitronics Corp. v. Conceptronic, Inc., 36 F. Supp. 2d 440, 441 (D. N.H. 1997). The Federal Circuit is the proper forum to resolve conflicts between this court's claim construction and the Board's claim construction.[2]

B. The Board's Claim Construction Is Not Persuasive

The patent terms at issue describe connections in the multiplexer circuit between the input and output terminals. One of the patent terms states, "one of the fourth stage input terminals coupled to the third stage output terminal." Two other patent terms are similar except that they describe the

---

[2] District courts apply different standards than the Board in construing patent claims. The court must construe claims in light of the statutory presumption that an issued patent is valid, while in reexamination proceedings the Board interprets patent claims as broadly as reasonably possible. See In re Etter, 756 F.2d 852, 855-59 (Fed. Cir. 1985) (en banc).

connections between the third stage input terminal and the second stage output terminal, and between the second stage input terminal and the first stage output terminal.

In construing these claims, the Special Master thoroughly analyzed the effect of intermediate outputs:

> One could argue endlessly over fine points like whether a "signal" that is output to inactive circuitry performs any function at all, or whether outputting a value to circuitry that is incapable of processing that value can really be regarded as coupling that value to an input of that circuitry. In the view of the S[pecial] M[aster], the only rational way to approach this problem is by looking at each claim as a whole. When this is done, it is seen that the claim defines a multiplexer circuit, and if the TGM stages are hooked up as recited in the remainder of the claim, the result will be a N:1 multiplexer circuit. The question then becomes: Does an intermediate output branching off to other circuitry destroy the character of the circuit as an N:1 multiplexer? Plaintiff concedes that it does where the other circuitry generates an output value. But is this so when the other circuitry does nothing with that intermediate output? In the view of the SM, this is a classic factual question of infringement. Experts can undoubtedly be of assistance to the Court and the jury in deciding whether a particular instance of intermediate branching does or does not result

> in something that can be regarded as an N:1 multiplexer circuit.

This court adopted the Special Master's recommended construction, and interpreted the term in part as follows:

> This means that the third stage output terminal cannot also be coupled to other circuitry such that the overall result is not a N:1 multiplexer circuit.

The Board considered this claim construction to be incomplete. The Board added its own interpretation, which defendants now contend this court should adopt:

> However, a multiplexer structure does not cease to become a multiplexer because of the way the intermediate and/or final TGM outputs are connected to surrounding circuitry. Therefore, we interpret this limitation to not preclude coupling the third stage output terminal to other circuitry.[3]

The Board's most recent claim construction does not require reconsideration. As the Special Master stated, "the claim limitation does not preclude intermediate outputs unless the presence of such an output would result in a circuit that is not a multiplexer. These ultimate determinations are

---

[3] The Board considered its claim construction on this issue to be dictum, stating that "[t]his difference in interpretation plays no part in the decision."

factual questions of infringement." (Emphasis added.) I have previously explained why the jury was to resolve the dispute over intermediate outputs:

> Here, the jury was instructed that a "multiplexer" was a "circuit that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals." The jury was instructed that the phrase "one of the second stage input terminals coupled to the first stage output terminal" "means that the first stage output terminal cannot also be coupled to other circuitry such that the overall result is not a N:1 multiplexer circuit." The jury received analogous instructions that the second and third stage output terminals cannot also be coupled to other circuitry if the result would not be a N:1 multiplexer circuit. The jury heard conflicting expert testimony on whether the prior art circuits cited by defendants as anticipatory were N:1 multiplexer circuits.
>
> . . . .
>
> Similarly, plaintiff presented substantial evidence that the prior art adder circuits cited by defendants used "live" intermediate outputs that were necessary to their function as adder circuits. The jury could reasonably find that because of the live intermediate outputs, the adder circuits cited by defendants operated effectively as 4:3 or 5:4

circuits, rather than 4:1 or 5:1 multiplexer circuits.

The parties presented conflicting evidence on this issue at the validity trial. Both the inventor and plaintiff's expert testified that prior art circuits which used live intermediate outputs did not function as N:1 multiplexers. Defendants presented expert testimony to the contrary. The verdict indicates that the jurors agreed with plaintiff's position.

The effect of live intermediate outputs presented a factual issue for the jury to resolve. I do not adopt the Board's most recent claim construction on the effect of intermediate outputs.

As another ground for reconsideration, defendants cite a recent Federal Circuit decision on claim construction, Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir.) (en banc), petition for cert. filed, 74 U.S.L.W. 3308 (U.S. Nov. 9, 2005) (No. 05–602). In Phillips, the court criticized Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193 (Fed. Cir. 2002), as allowing a court construing patent claims to adopt dictionary definitions of the words used in a patent claim "entirely divorced from the context of the written description." 415 F.3d at 1321.

The Special Master did discuss the Texas Digital opinion in his initial report and recommendation on claim construction. In summarizing the holding of Texas Digital, the Special Master stated, "By examining relevant dictionaries, encyclopedias and treatises to ascertain possible meanings that would have been attributed

to the words of the claims by those skilled in the art, and by further utilizing the intrinsic record to select from those possible meanings the one or ones most consistent with the use of the words by the inventor, the full breadth of the limitations intended by the inventor will be more accurately determined and the improper importation of unintended limitations from the written description into the claims will be more easily avoided." However, the Special Master also noted that the specification is the "single best guide to the meaning of a disputed term," a statement that is in accord with Phillips. See 415 F.3d at 1315 (emphasizing importance of the specification).

The Special Master's claim construction was not "entirely divorced" from the written description. The Special Master thoroughly analyzed all relevant evidence in arriving at his construction of the terms of the patent claims. The Phillips opinion's partial repudiation of Texas Digital does not justify revisiting claim construction.

Because I deny defendants' motion for reconsideration on the merits, I do not address plaintiff's argument that defendants are judicially estopped from raising these issues.

III. Defendants' Motion for Partial Reconsideration of Claim Construction Order and Motion for New Trial on Validity

Defendants move for an order under Federal Rule of Civil Procedure 54(b) correcting this court's claim construction. Defendants again rely on the Board's most recent claim construction, arguing that

"[t]his Court should construe the claim in the same way the [Board] construed it."

The Board interpreted the term "coupled to receive" as "terminal capable of receiving." I agree with plaintiff that the Board's construction of "coupled to receive" is not persuasive. The term "coupled" implies a connection, while the Board's construction of "coupled" as "capable of receiving" would not necessarily require an actual connection.

Defendants cite the Board's determination that "input variables" and "control signals" are not part of the claimed structure of the '666 Patent. Although the signals themselves may not be part of the claimed structure, the input terminals that receive the signals are part of the claimed structure. There was sufficient evidence at trial from which a reasonable jury could find that prior art circuits which did not allow the reception of four or five different input variables did not anticipate claims 16 or 17 of the '666 Patent. Similarly, a reasonable jury could find that prior art circuits which were not coupled to allow three or four different control input signals did not anticipate.

I deny defendants' motion for partial reconsideration. I deny plaintiff's motion to strike the motion to reconsider.

CONCLUSION

Defendants' motions for judgment as a matter of law on inducement (#780), for reconsideration on anticipation (#815), and for partial reconsideration of claim construction (#826) are denied.

DATED this 13 day of December, 2005.

/s/ Owen M. Panner

OWEN M. PANNER
U.S. DISTRICT JUDGE

APPENDIX D

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed DEC 13, 2005]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Civil Action No.: 3-99-00407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	FINAL JUDGMENT
Defendants.	)	

Kevin M. Hayes, OSB 01280
Jeffrey S. Love, OSB No. 87398
John D. Vandenberg, OSB No. 89375
KLARQUIST SPARKMAN, LLP

David Axelrod
Schwabe, Williamson & Wyatt, PC
Pacwest Center
Suite 1600-1800
1211 SW Fifth Avenue
Portland, OR 97204-3795

One World Trade Center
Suite 1600
121 S.W. Salmon Street
Portland, Oregon
97204-2988

Attorneys for Plaintiff

Nathan Lane III
David S. Elkins
Squire, Sanders & Dempsey
One Maritime Plaza, Third Floor
San Francisco, CA
94111-3492

Attorneys for Defendants

PANNER, J.

Based on the jury verdict entered October 29, 2003 finding Claims 16 and 17 of U.S. Patent No. 5,162,666 not invalid for obviousness or anticipation, the Court's order entered February 22, 2005 finding on summary judgment that certain SH microprocessors infringe Claims 16 and 17 of the Patent, the jury verdict entered May 10, 2005 finding that Hitachi, Ltd. induced certain third parties to infringe the Patent and awarding Plaintiff $86.5 million in damages against all Defendants, the stipulations filed by the Parties and the Court's file herein,

IT IS HEREBY ADJUDGED AND DECREED that:

1. Plaintiff is the owner of U.S. Patent No. 5,162,666.

2. Claims 16 and 17 of U.S. Patent No. 5,162,666 are not invalid.

3. Hitachi America, Ltd. and Renesas Technology America, Inc. infringed Claims 16 and 17

of U.S. Patent No. 5,162,666 under 35 U.S.C. §271(a).

4. Hitachi, Ltd. infringed Claims 16 and 17 of the Patent under 35 U.S.C. §271(b).

5. Plaintiff's claims against Hitachi, Ltd. for direct infringement under 35 U.S.C. §271(a) and for actively inducing infringement by SuperH, Inc., Compaq Computer, Xybernaut Corporation, and Snapgear, Inc. are dismissed without prejudice.

6. Plaintiff's claims of willful infringement, and its claim of infringement as to SH-3 microprocessor model number HD6417096S, are dismissed with prejudice.

7. Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. are jointly and severally liable to Plaintiff for damages in the amount of $86,500,000.

8. Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. are jointly and severally liable to Plaintiff for costs in an amount to be fixed by the Court after entry of judgment and for prejudgment interest on the $86,500,000 in damages in the amount of $18,189,434, plus $11,018 per day for each day after June 11, 2005, until the final judgment is entered.

9. The Court retains jurisdiction of this case for purposes of enforcing the permanent injunction previously entered, including any discovery related thereto.

10. Post-judgment interest shall accrue on any unpaid amounts from the date this judgment is entered until full satisfaction, as provided in 28 U.S.C. §1961.

Dated this 13 of Dec, 2005.

/s/ Owen M. Panner

OWEN M. PANNER
U.S. DISTRICT JUDGE

APPENDIX E

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed May 6, 2005]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Civ. No. 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	VERDICT FORM
Defendants.	)	

We the jury, being duly empaneled, find as follows:

1. Did Hitachi, Ltd. induce one or more of the companies below to import into the United States, or to use, offer for sale in, or sell in the United States, accused products containing SH

microprocessors that infringe claims 16 and 17 of plaintiff's U.S. Patent No. 5,162,666:

Sega Enterprises, Ltd., of Japan — Yes X — No ___

Casia Computer Co., Ltd., of Japan — Yes X — No ___

2. Enter below the amount of damages you find that plaintiff has suffered as a result of defendants' infringement of claims 16 and 17 of plaintiff's U.S. Patent No. 5,162,666, up to today:

$ 86,500,000.00

Dated this 6 Day of May 2005.

Signed: /s/ [ILLEGIBLE]

Presiding Juror

APPENDIX F

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed FEB 22, 2005]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	CV 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	ORDER
Defendants.	)	

PANNER, J.

Plaintiff Translogic Technology, Inc. brings this action for patent infringement against defendants Hitachi Ltd., Hitachi America, Ltd., and Renesas Technology America, Inc. Plaintiff contends that defendants' products infringe plaintiff's U.S. Patent No. 5,162,666 (the '666 Patent), for a transmission gate series multiplexer.

The special master has issued his report and recommendation on infringement. The parties object to the report. After de novo review, I adopt the special master's recommendations, except that I conclude plaintiff is entitled to summary judgment on the reverse doctrine of equivalents.

BACKGROUND

The special master recommends that:

(1) the accused circuits are multiplexer circuits satisfying the multiplexer limitation of claims 16 and 17;

(2) the accused circuits use "input variables" and "control signals," and satisfy those limitations in claims 16 or 17;

(3) genuine issues of fact exist regarding whether certain accused circuits, termed Circuit Path Type Parallel, meet the limitation of "stage" as construed by the court;

(4) genuine issues of fact exist regarding whether defendants configured accused circuit SH7727, paths 2-9, 11-13, 15-52, and 56-58, so that the final stage does not work as a TGM;

(5) except for the circuits mentioned in (3) and (4), the accused circuits literally infringe the '666 Patent because they meet all the limitations of either claim 16 or 17;

(6) genuine issues of fact exist regarding defendants' assertion of the reverse doctrine of equivalents.

STANDARDS

If a party objects to findings of fact or legal conclusions in a special master's report and recommendation, the court reviews the disputed issues de novo. Fed. R. Civ. P. 53(g).

DISCUSSION

I. Plaintiff's Objections

A. The Reverse Doctrine of Equivalents

Plaintiff objects to the special master's sixth recommendation that material issues of disputed fact preclude summary judgment on defendants' affirmative defense of the reverse doctrine of equivalents. I conclude that plaintiff is entitled to summary judgment on this affirmative defense.

Under the reverse doctrine of equivalents, an accused product that falls within the literal words of a patent claim may avoid infringement if the accused product "is so far changed in principle that it performs the same or similar function in a substantially different way." Graver Tank & Mfg. Co. v. Linde Air Prods. Co., 339 U.S. 605, 608-09 (1950). The reverse doctrine applies only when the accused product, although literally infringing, has been so changed that it is no longer the invention disclosed by the patent. See Report at 35.

The reverse doctrine of equivalents is an affirmative defense and the defendant bears the burden of proof by a preponderance of the evidence. SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 1123-24 (Fed. Cir. 1985) (en banc). "If the accused

infringer makes a prima facie case, the patentee, who retains the burden of persuasion on infringement, must rebut that prima facie case." Id. (citations and footnote omitted). The fact question presented by the reverse doctrine "is simple and direct: Is the accused product so far changed in principle that it performs the function of the claimed invention in a substantially different way?" Id. at 1124.

Here, defendants have not presented evidence that the accused circuits perform the function of the plaintiff's invention in a substantially different way. Id. Like the serial multiplexers in claims 16 and 17 of the '666 Patent, the accused circuits select one output signal from either four or five inputs, using a serial arrangement of transmission gate multiplexers. I grant summary judgment for plaintiff on the affirmative defense of the reverse doctrine of equivalents.

B. Parallel Circuits

In his third recommendation, the special master found genuine issues of material fact whether certain accused circuits, referred to as "Circuit Path Type Parallel," meet the limitation of "stage." If the "stages" of these accused circuit paths contain more than "a single TGM circuit," then they would not literally infringe claims 16 and 17.

While objecting to this finding, plaintiff seeks to withdraw its claims against this category of circuits. I allow plaintiff to withdraw these claims without prejudice.

C. Configuration of the SH7727 Circuit

In his fourth recommendation, the special master concluded that there were genuine issues of fact regarding accused circuit SH7727 paths 2-9, 11-13, 15-52, and 56-58. Defendants allege that they configured these circuit paths before shipping to the United States so that the final stage would not work as a TGM.

Plaintiff objects. I agree with the special master that material issues of disputed fact preclude summary judgment on this issue. Cf. Intel Corp. v. United States ITC, 946 F.2d 821, 832 (Fed. Cir. 1991).

II. Defendants' Objections

Defendants object to the special master's fifth recommendation that the accused circuits, with the limited exceptions noted in recommendations 3 and 4, literally infringe claims 16 and 17 of the '666 Patent. Defendants contend that

(1) judicial estoppel bars plaintiff from taking its current position on surrounding circuitry because plaintiff took a different position at the validity trial;

(2) the "select-to-select" circuit paths do not meet the "control signal" limitation of claims 16 and 17; and

(3) accused circuit paths of the SH7750 microprocessor have more than one TGM per stage and therefore do not infringe.

I adopt the special master's fifth recommendation that the accused circuits, with the

exceptions noted, literally infringe claim 16 or 17, or both. The special master's report clearly and comprehensively explains why the accused products literally infringe.

I also agree with the report that judicial estoppel does not bar plaintiff's arguments because plaintiff has not taken inconsistent positions. Defendants' other objections to the special master's recommendations are without merit.

CONCLUSION

On de novo review, the special master's report and recommendation on infringement (#564) is adopted except as to the reverse doctrine of equivalents. Plaintiff's motion for summary judgment (#443) is granted as to infringement and otherwise denied at this time.

IT IS SO ORDERED.

Dated this 22 day of February, 2005.

/s/ Owen M. Panner

OWEN M. PANNER
U.S. DISTRICT JUDGE

APPENDIX G

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Case No. CV 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	
Defendants.	)	

REPORT AND RECOMMENDATION
OF SPECIAL MASTER
REGARDING INFRINGEMENT

This case involves an assertion of infringement by defendants of claims 16 and 17 of U.S. Patent No. 5,162,666, which is owned or controlled by plaintiff.

In an order dated July 31, 2003, the Court appointed the undersigned as Special Master (SM) pursuant to Rule 53, FRCP. The specific purpose of that reference was to make recommendations to the Court regarding the construction of the claim terms at issue. A Markman hearing[1] was held and the SM filed two reports: Report and Recommendation of Special Master Regarding Claim Construction (Report I) and Second Report and Recommendation of Special Master Regarding Claim Construction (Report II). The Court adopted the recommendations set forth in those reports (see Order of October 6, 2003), and used them as the basis for an instruction on claim construction that was provided to the jury during a trial of the invalidity defenses in October, 2003. The jury concluded that claims 16 and 17 were not invalid for anticipation or obviousness, and its verdict has survived motions for JMOL and new trial. (See Opinion and Order of February 9, 2004.)

In an order dated August 27, 2004, the Court again referred this matter to the SM "to issue a report and recommendations on pending infringement issues." The basic vehicle for resolution of the infringement issues is "Plaintiff's Motion for Summary Judgment of Infringement and Permanent Injunction." The motion seeks a summary judgment that claims 16 and 17 are directly infringed by some 344 accused circuits[2]

---

[1] See Markman v. Westview Instr., Inc., 52 F.3d 967, 34 USPQ2d 1321 (Fed. Cir. 1995), aff'd 517 U.S. 370, 38 USPQ2d 1461 (1996).

[2] Plaintiff accused 348 circuits, but has conceded that circuit paths 44 and 45 in the SH7290 and SH7290R microprocessors

(...continued)

embodied in 18 Hitachi microprocessors. Inasmuch as a motion for summary judgment is involved, the August 27 order of reference also provides that the "special master shall identify any issues of material fact that cannot be resolved as a matter of law, and may provide his suggestions for resolving those issues." See Rule 56(d), FRCP.

Defendants have also filed a summary judgment motion, seeking (among other things) a partial summary judgment of noninfringement as to 8 of the 18 accused microprocessors on the ground that they "have not been made, used, sold or offered for sale in or imported into this country by any defendant." In other words, regardless of whether claims 16 and 17 cover circuits in those microprocessors, there is no liability for infringement, according to defendants. Resolution of defendants' motion is beyond the scope of the August 27 reference. Accordingly, for purposes of the present report, it will be assumed that the microprocessors in question were used in this country.

It should also be noted that defendants have not filed a cross-motion for summary judgment in response to plaintiff's motion. Nonetheless, the parties are agreed that, in the event the SM should conclude, as a matter of law, that plaintiff has been unable to demonstrate infringement in one or more instances, a recommendation of judgment of

---

do not infringe, thus reducing the total to 344. See footnote 4 of plaintiff's summary judgment reply brief.

noninfringement in those instances would be appropriate. This also seems consistent with the language of the August 27 order.[3] Clearly, a district court has the power to enter summary judgment sua sponte, without the need for a cross-motion by the prevailing party.[4]

DISCUSSION

Proceedings on Plaintiff's Motion

This matter has been extensively briefed by the parties. Plaintiff's original memorandum in support of its motion (PB-I) was submitted February 11, 2004, together with its concise statement of material facts (PS) and several supporting declarations and expert reports.[5] Defendants' responsive memorandum (DB-I) and concise statement of material facts (DS) were submitted April 20, 2004; these too were accompanied by supporting declarations and reports.[6] On May 5,

---

[3] "The final report and recommendations shall, to the extent possible, contain conclusions on whether each accused circuit infringes claim 16 or claim 17 of the '666 Patent."

[4] See Celotex Corp. v. Catrett, 477 U.S. 317, 326 (1986); International Visual Corp. v. Crown Metal Mfg. Co., 991 F.2d 768, 26 USPQ2d 1588, 1590 (Fed. Cir. 1993).

[5] These include first (RD-I) and second (RD-II) declarations of plaintiffs expert, Russell Randolph, and his expert report (RR).

[6] These include expert declarations of Carl Sechen and Harry Tredennick. Defendants have since submitted restated expert reports and second declarations for both experts. Unless otherwise indicated, all references herein will be to their second

(...continued)

2004, plaintiff submitted a reply memorandum (PB-II). Between them, the parties have proffered the October 2003 trial transcript, many of the exhibits, expert reports, and other materials they feel may be relevant to the task at hand.

Inasmuch as 344 separate circuits are accused to infringe, that task can be viewed as somewhat daunting. In recognition of this prospect, the August 27 order of reference directed the parties to meet and "attempt to agree on the accused circuits that will serve as representative circuits for the special master's analysis. If the parties cannot agree, the special master will select representative circuits." The parties met on September 10, 2004, but were unable to agree on representative circuits. A telephone conference pursuant to Rule 53(d)(1), FRCP, was held September 20. During that conference the SM concluded that written statements on the question of representative circuits would facilitate selection. Accordingly, the parties submitted simultaneous proposals (PB-III & DB-II) on September 24 and responses (PB-IV & DB-III) on October 1.

The Court's August 27 order provided, in paragraph 5, that the SM "shall prepare a proposed report and recommendations on the infringement issues and provide it to the parties with a schedule for receiving the parties' comments. The special master shall then prepare and deliver the final

---

declarations (i.e., SD-II & TD-II) and restated reports (i.e., SR II & TR-II).

report and recommendations to the court and the parties." In a letter emailed to the parties on September 28, the SM advised them that, in light of their submissions of September 24 and October 1, he would be in a position to prepare and issue a proposed report without the need for further briefing.[7] On October 2, 2004, the SM emailed a "Proposed Report and Recommendation of Special Master Regarding Infringement." In keeping with paragraph 5 of the August 27 order, the parties were invited to comment.

A round of substantive briefing ensued, directed largely at the content of the SM's proposed report. The parties submitted briefs (PB-V & DB-IV) on November 1, 2004, and responses (PB-VI & DB-V) on November 15, 2004.[8] A hearing was held in Chicago, Illinois on December 2, 2004.

Representative Circuits

As indicated above, the parties were unable to agree upon a selection of representative circuit paths. As will become apparent later in this report, in view of the SM's recommended disposition of the

---

[7] The submissions on selection of representative circuits contained extensive exposition and argument of the substantive infringement issues; these were sufficient to enable the SM to reach tentative conclusions and prepare a proposed report for circulation to the parties.

[8] Submitted with DB-IV were a Supplemental Declaration of Tredennick (TD-III) and a Declaration of Toshihiro Hattori (HD); a Second Supplemental Declaration of Tredennick (TD-IV) accompanied DB-V.

various issues at hand, a selection of representative circuits turned out to be neither necessary nor useful.[9] Nonetheless, some basic categorization of the 344 separate circuit paths that are accused to infringe will facilitate the following discussion.

In his restated report (SR-II), defendants' expert Sechen undertook a comprehensive categorization, resulting in five circuit types: DD, SS, DS, DO, and Parallel.[10] The accused circuit paths, identified by Hitachi SH product number, and path number, are grouped according to these categories in Exhibit B to DB-II. It should be noted that some paths are assigned to more than one category.[11]

For the limited purposes of this report, Sechen's categorization is reasonable and workable. Indeed, plaintiff does not object to Sechen's categorization per se; its opposition has to do with the selection of representative circuit paths from

---

[9] But see the discussion of the Hattori Declaration in connection with the "Multiplexers vs. Logic Circuits" issues.

[10] The letter designations are apparently shorthand for certain signal dependencies that Sechen contends are present in the circuit paths: i.e. data-to-data (DD), select-to-select (SS), data-to-select (DS), and data-to-output (DO). (TD-III ¶7) The "Parallel" designation reflects his contention that certain circuit paths contain more than one TGM per stage.

[11] For example, SH7190 Paths 1-16 are assigned to Path Types DD and DS.

those categories.[12] It should simply be understood that adoption of his categories as a means of conveniently grouping certain identified circuit paths says nothing about the merits of the underlying controversy.

Accordingly, when accused circuit paths are referred to in this report by type, it will be understood that the reference is to the categorization set forth in Exhibit B to DB-II.[13]

Summary Judgment Fundamentals

Summary judgment is as appropriate in a patent case as it is in any other case. A motion for summary judgment is properly granted only where the pleadings, depositions, answers to interrogatories, and admissions on file, together with any affidavits, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law. The party moving for summary judgment carries the burden of

---

[12] "Defendants' proposed circuit categories would be fine, if Defendants would clear limit their arguments to points applicable to all circuits within their categories. They have not done that, at least not clearly." (PB-IV at 1)

[13] There is one significant controversy about the categorization reflected in Exhibit B. Defendants' expert Tredennick avers that he has "updated" his Exhibit 4. (TD-III ¶12) Defendants characterize this "updating" to the effect that "Exhibit 4 now shows some additional circuit paths that should be properly be included in the 'parallel' category type." (DB-IV at 2) This controversy is examined in connection with the "More Than One TGM Per Stage" discussion below.

demonstrating the absence of any genuine issue of material fact and its entitlement to judgment as a matter of law. In ruling on a motion for summary judgment, the district court is required to view the evidence presented in a light most favorable to the nonmoving party and to draw all reasonable inferences in favor of the nonmoving party. However, the nonmoving party must do more than simply present some evidence as to an issue it asserts is in dispute. Rather, the standard is that sufficient evidence must be forthcoming such as would allow a reasonable jury to return a verdict in favor of the nonmoving party.[14]

The inquiry involved in a ruling on a motion for summary judgment necessarily implicates the substantive evidentiary standard of proof that would apply at the trial on the merits.[15] Infringement, literal or by equivalents, requires proof by a preponderance of the evidence.[16] Though literal infringement of a properly interpreted claim is a fact question, its determination may be rendered clearly erroneous through an improper interpretation and application of the governing law.[17]

---

[14] E.g., C.R. Bard Inc. v. Advanced Card. Sys. Inc., 911 F.2d 670, 15 USPQ2d 1540, 1542 (Fed. Cir. 1990).

[15] E.g., Baker Oil Tools, Inc. v. Geo Vann, Inc., 828 F.2d 1588, 4 USPQ2d 1210, 1215 (Fed. Cir. 1987).

[16] E.g., Lemelson v. United States, 752 F.2d 1538, 224 USPQ 526, 531 (Fed. Cir. 1985).

[17] Amstar Corp. v. Envirotech Corp., 730 F.2d 1476, 221 USPQ 649, 653 (Fed. Cir. 1984).

Early on, the Federal Circuit expressed itself quite clearly on the subject of summary judgment as it relates to the issue of infringement:

> It is at least conceivable that comparison of a properly interpreted claim with a stipulated or uncontested description of an accused device or process would reflect such an absence of material fact issue as to warrant summary judgment of infringement or noninfringement. Because infringement is itself a fact issue, however, a motion for summary judgment of infringement or noninfringement should be approached with a care proportioned to the likelihood of its being inappropriate.[18]

To prevail here on summary judgment, plaintiff is thus obligated to demonstrate, without intrusion of genuine issues of material fact, that claims 16 and 17, as interpreted by the court, read literally[19] on the 344 accused circuits.

Plaintiff's Burden

Both sides are faced with essentially the same ultimate burden in seeking a summary judgment with respect to infringement. As the Federal Circuit sees it, "[a]n infringement issue is properly decided upon summary judgment when no reasonable jury

---

[18] D.M.I. Inc. v. Deere & Co., 755 F.2d 1570, 225 USPQ 236, 238 (Fed. Cir. 1985).

[19] Plaintiff says that it "has not moved for summary judgment under the doctrine of equivalents (reserving that issue for trial if this motion is denied)." (PB-II at 6)

could find that every limitation recited in the properly construed claim either is or is not found in the accused device either literally or under the doctrine of equivalents."[20] Plaintiff, as the patent owner, has the burden of going forward, and the ultimate burden of persuasion by a preponderance, on the issue of infringement. Under modern summary judgment law, a patentee who fails to provide probative evidence of infringement runs the risk of being peremptorily nonsuited. Evidence from which a reasonable fact-finder could find infringement will forestall this possibility. However, a party does not meet this evidentiary threshold merely by submitting the affidavit of an expert who opines that the accused device meets the claim limitations.[21] In the summary judgment context, the expert must set forth the factual foundation for his or her opinion – such as a statement regarding the structure found in the accused product – in sufficient detail for the court to determine whether that factual foundation would support a finding of infringement under the claim construction adopted by the court, with all reasonable inferences drawn in favor of the nonmovant.[22]

I have examined plaintiff's submissions with these rules in mind. That examination has yielded a

---

[20] Gart v. Logitech Inc., 254 F.3d 1334, 59 USPQ2d 1290, 1293 (Fed. Cir. 2001).

[21] Novartis Corp. v. Ben Venue Labs. Inc., 271 F.3d 1043, 60 USPQ2d 1836, 1841-42 (Fed. Cir. 2001).

[22] Arthur A. Collins Inc. v. Northern Telecom Ltd., 216 F.3d 1042, 55 USPQ2d 1143, 1147 (Fed. Cir. 2000).

firm conviction on my part that plaintiff has successfully completed the first step in its quest for a summary judgment of literal infringement for all of the 344 accused circuits. The carefully documented declarations of its expert, Randolph, contain adequate provenance of the structure of the accused circuits, and a methodical and reasonable exposition of why he believes that the circuits contain structure that corresponds to the claim limitations as construed by the Court.

Mr. Randolph's first declaration, dated December 29, 2003, identifies schematic drawings of the accused circuits that he prepared based upon information provided by defendants, and expresses the opinion that those circuits meet all the limitations of claims 16 and 17 as construed by the Court. (RD-I ¶2) His second declaration, dated February 2, 2004, identifies a set of schematic drawings that were produced by defendants on January 20, 2004. (RD-II ¶2 & Ex. 2) He attaches a number of these drawings, marked with his blue notations, and states that the drawings confirm his prior opinion that the accused circuits meet all of the limitations of either claim 16 or 17. (RD-II ¶2 & Ex. 1) He includes a table that provides a limitation-by-limitation comparison of claim 16 with the accused 4:1 multiplexer circuits, and indicates that the analysis would be essentially identical for claim 17 and the accused 5:1 circuits. (RD-II ¶4) In his report, dated February 9, he explains how he extracted the schematic circuit diagrams from the information produced by defendants (RR ¶¶11-14) and again states that the Hitachi drawings produced on January 20 confirm his opinions as to literal claim readability. (RR ¶¶21-28 & 31)

Defendants and their experts do not appear to question the accuracy of Randolph's circuit extraction. Indeed, in his first report, Sechen assumed that Randolph's work was accurate, and found a benefit in using Randolph's diagrams:

> 9. Randolph had already completely extracted each GDSII file for all of the specified SH microprocessors, thus yielding hierarchical spice netlists for each of the microprocessors. To verify that Randolph had done this correctly, we also extracted blocks from a couple of microprocessors from the GDSII files (also yielding hierarchical spice netlists) and *were able to verb Randolph's extractions by running a netlist comparison program called Gemini.* We therefore assume that Randolph's extraction (which he obtained simply by running a Mentor Graphics extraction program) were correct, and thus decided to base our path analysis on Randolph's extracted hierarchical spice netlists. The *clear advantage in doing so* is that then the instance and net names we are dealing with in the extraction will exactly match those in the paths specified by Randolph. (SR-I ¶9; emphasis added)

In his restated report, Sechen does not repeat this concession, but he does not retract it either. He states that the extraction "are a higher-level abstraction of what's really on the integrated circuits, and certainly they do not illustrate every or even most aspects of the actual integrated circuit." Nonetheless, he concedes that "[t]hey do, however, allow one to analyze the approximate behavior of the

microprocessor." (SR-II ¶13) Thus, he indicates that his analysis was based on "the *circuit paths* identified by Randolph on the extracted hierarchical spice netlists he provided." (SR-II ¶14; emphasis present) He then proceeds to opine that Randolph's circuit paths were incomplete, in a way that "did not show crucial dependences between the various signals on the paths." (SR-II ¶15) (This objection will be discussed in detail later.) He also points out that neither the circuit paths provided by Randolph, nor the circuit diagrams produced by defendants, are "representations of actual circuits as implemented in the final microprocessor." (Ibid) This may be so, but it is hardly a reason to reject the diagrams as being an incorrect illustration of what they purport to show. The diagrams may be high-level depictions of the accused circuitry, but they are surely no more so than the illustrative drawings in the '666 patent. Moreover, defendants can scarcely complain about Randolph using *their own diagrams* as a basis for his analysis.

I have also examined the first and second Tredennick declarations and his original and restated expert reports. Tredennick, like Sechen, does not appear to take issue with the diagrams used by Randolph. In the end, defendants' real quarrel with Randolph's analysis is not that it was based upon inaccurate information, but that it failed to take into account additional information that defendants' experts think is crucial and Randolph thinks is irrelevant.

Defendants' Burden

The declarations and other evidence submitted by plaintiff would therefore, if unopposed, establish its right to summary judgment of literal infringement. To avoid that result, defendants here are required merely to point to an evidentiary conflict created on the record,[23] although general assertions of fact issues, general denials, and conclusory statements are insufficient to shoulder a non-movant's burden.[24] Of course, defendants' evidence is to be believed and all justifiable inferences are to be drawn in their favor.[25]

My review of the Sechen and Tredennick declarations, along with the other evidence submitted by defendants, likewise convinces me that defendants have provided adequate technical and logical foundation for the factual opinions professed by those experts. Those opinions, if unopposed by plaintiff, would result in a conclusion that, at the very least, genuine issues of material fact remain to be tried.

But plaintiff does oppose the opinions of defendants' experts, and the only way to determine whether *either side* is entitled to summary judgment

---

[23] Armco Inc. v. Cyclops Corp., 791 F.2d 147, 229 USPQ 721, 722 (Fed. Cir. 1986).

[24] Chemical Eng'g Corp. v. Essef Indus. Inc., 795 F.2d 1565, 230 USPQ 385, 390 (Fed. Cir. 1986).

[25] Monsanto Co. v. Bayer Bioscience N.V., 363 F.3d 1235, 70 USPQ2d 1257, 1261 (Fed. Cir. 2004).

with respect to any or all of the accused circuits is to consider, one-by-one, defendants' contentions and plaintiff's responses thereto. The essential positions of the parties can be summarized like this: defendants have been able to establish genuine issues of fact in several respects; plaintiff says those factual issues are not *material* to the question of literal infringement.

Judicial Estoppel

At the outset, it is necessary to consider some aspects of the equitable doctrine of judicial estoppel. Defendants have raised the question of judicial estoppel by pointing to several instances where plaintiff's witnesses testified (or plaintiff's counsel argued) during the validity trial and elsewhere in a way that defendants contend is clearly inconsistent with plaintiff's current position on infringement.

The court that will have jurisdiction of any appeal in the present litigation, the Federal Circuit, applies regional circuit law to questions of judicial estoppel.[26] That court has noted that the doctrine of judicial estoppel may not be followed by anything

---

[26] E.g., U.S. Philips Corp. v. Sears, Roebuck & Co., 55 F.3d 592, 34 USPQ2d 1699, 1703 n.3 (Fed. Cir. 1995) (Seventh Circuit law); Wang Labs., Inc. v. Applied Computer Sci., Inc., 958 F.2d 355, 22 USPQ2d 1055, 1058 (Fed. Cir. 1992) (First Circuit law). Nonetheless, it appears to apply its own law to the doctrine of preclusion of inconsistent positions, which to the SM is virtually indistinguishable from judicial estoppel. See Hybritech Inc. v. Abbott Labs., 849 F.2d 1446, 7 USPQ2d 1191, 1197-98 (Fed. Cir. 1988).

approaching a majority of jurisdictions, nor is there a discernable modem trend in that direction.[27] Ninth Circuit law on the subject is exemplified by a very recent case.[28] The Supreme Court's most recent pronouncement on the subject is apparently New Hampshire v. Maine.[29] In that case, the Court did not trouble itself to explain what law it was applying; indeed, inasmuch as the case was one within the Court's original jurisdiction, it was perhaps content to apply its own law (if that phrase has a meaning in our Federal system). At any rate, it would be folly to ignore New Hampshire v. Maine in sorting out the judicial estoppel issues in the present case, for Supreme Court law binds everybody involved in a federal matter, from the Ninth and Federal Circuits all the way down to the SM and the parties. The Court summarized the doctrine this way:

> This rule, known as judicial estoppel, "generally prevents a party from prevailing in one phase of a case on an argument and then relying on a contradictory argument to prevail in another phase."
>
> *** [C]ourts have uniformly recognized that its purpose is "to protect the integrity of the judicial process," by "prohibiting parties from deliberately changing positions according

---

[27] Water Techs. Corp. v. Calco. Ltd., 850 F.2d 660, 7 USPQ2d 1097, 1101 n.4 (Fed. Cir. 1988).

[28] Wagner v. Professional Engineers in Calif. Gov't, 354 F.3d 1036 (9th Cir. 2004).

[29] 532 U.S. 742 (2001).

to the exigencies of the moment," Because the rule is intended to prevent "improper use of judicial machinery," judicial estoppel "is an equitable doctrine invoked by a court at its discretion."

*** [S]everal factors typically inform the decision whether to apply the doctrine in a particular case: First, a party's later position must be "clearly inconsistent" with its earlier position. Second, courts regularly inquire whether the party has succeeded in persuading a court to accept that party's earlier position, so that judicial acceptance of an inconsistent position in a later proceeding would create "the perception that either the first or the second court was misled." Absent success in a prior proceeding, a party's later inconsistent position introduces no "risk of inconsistent court determinations," and thus poses little threat to judicial integrity. A third consideration is whether the party seeking to assert an inconsistent position would derive an unfair advantage or impose an unfair detriment on the opposing party if not estopped.

In enumerating these factors, we do not establish inflexible prerequisites or an exhaustive formula for determining the applicability of judicial estoppel. Additional considerations may inform the doctrine's

application in specific factual contexts.[30] [All citations omitted.]

In the present case, the most significant of the enumerated factors is the first – that the testimony or argument be clearly inconsistent with plaintiff's current position on infringement. That inquiry will of course implicate the context – whether or not it was made in an effort to sustain the patent's validity, which was the subject of the trial. Contextual evaluation probably shades somewhat into the second factor – success in persuading the jury to accept plaintiff's position – although testimony of a witness that appears plainly designed to counter an attack on the validity of the patent must be presumed to have been successful, inasmuch as the jury verdict was that the patent was not invalid. The third factor is self-evident: a prior position resulting in a judgment that the patent is not invalid, coupled with a clearly inconsistent position resulting in a judgment of infringement, obviously imposes an unfair detriment on defendants.

Accordingly, in considering defendants' contentions about infringement, the primary focus in addressing their judicial estoppel argument will be an evaluation of whether the trial testimony was sufficiently inconsistent with plaintiff's present position in its motion for summary judgment of infringement to warrant a discretionary application of estoppel.

---

[30] Id. at 749-51.

With their November 1, 2004 brief, defendants also submitted a copy of an appeal brief that plaintiff filed in June of 2004 in connection with the reexamination of the '666 patent that is currently pending in the PTO.[31] This document was not available until after defendants had filed their April 20 brief (DB-I) in response to plaintiff's summary judgment motion. In any event, plaintiff raises no objection to consideration of this document, and it has been considered in connection with defendants' various arguments on judicial estoppel and admissions. It should be noted, however, that (insofar as the SM has been advised) the PTO has not acted on the appeal in the reexamination proceeding. Accordingly, the second New Hampshire v. Maine factor (success with respect to the earlier position) cannot be evaluated.

Tredennick's Summary

In his restated report, defendants' expert Tredennick undertakes a useful summary of defendants' essential contentions regarding literal infringement:

---

[31] Defendants included a formal Request for Judicial Notice, asking the SM and the Court to take notice of the appeal brief. The SM sees no reason why resort to the doctrine of judicial notice is necessary. The document has been authenticated satisfactorily and plaintiff has interposed no objection. The document evidences statements made by plaintiff to the PTO and is certainly appropriate for consideration on a motion for summary judgment.

> I have reviewed each of the accused Hitachi logic circuits. Each circuit fails for at least three reasons. First, each circuit fails at least one of the tests established to distinguish the claimed multiplexer from circuits in the prior art. Second, no accused circuit is NPN logically equivalent to a serial multiplexer. Third, each of the accused Hitachi logic circuits is similar to a least one prior-art circuit. (TR-II ¶57).

He appends a table (Updated Exhibit 4)[32] in which he summarizes his analysis of whether each accused circuit meets his criteria for literal infringement. Among these are whether it is a multiplexer, whether it has only one TGM per stage, whether the input variables can be one or zero at any given time, whether it has the required number of independent input variables and control signals, whether it is possible to exchange inputs, whether a tree-structured (parallel) multiplexer can be substituted for it, and whether it is NPN logically equivalent to a serial multiplexer. As will be seen, none of these criteria is material to the question of literal

---

[32] The original table was submitted as Exhibit 4 to Tredennick's restated report (TR-II). In his supplemental declaration accompanying DB-IV, he explains that he has updated Exhibit 4 "[i]n view of additional work undertaken by Dr. Sechen * * * and my own further analysis as set forth herein." (TD-III ¶12) All references herein will be to Updated Exhibit 4 unless otherwise indicated.

infringement, with the exception of whether the accused circuit has only one TGM per stage.[33]

It should be noted that Tredennick's table also analyzes whether the accused circuit is distinguishable from three prior art circuits: Ware's logic circuit, McAllister's logic circuit, and Ware's parallel TGM circuit. This provides the basis for his conclusion that "each of the accused Hitachi logic circuits is similar to at least one prior-art circuit." (TR-II ¶¶132, 141-42) Accepting, as we must for purposes of summary judgment, the truth of this conclusion, it too fails the legal test for materiality. In recently reaffirming that "practicing the prior art" is not a defense to literal infringement, the Federal Circuit had some things to say that are quite pertinent to the present case. After explaining that "literal infringement is determined by construing the claims and comparing them to the accused device, not by comparing the accused device to the prior art," and that "[p]rior art is relevant to literal infringement only to the extent that it affects the construction of ambiguous claims," the court went on to note:

---

[33] Certainly the overall question of whether the accused circuit is a multiplexer is material, but that is answered, in the view of defendants' experts, by evaluating the other criteria. E.g., "the accused circuits in Tredennick Ex. 3 cols. C and D do not have independent input signals or independent control signals or both. Consequently, the circuits that they form are *not multiplexers within the meaning of claims 16 and 17*." (DB-I at 24; emphasis added) See also the discussion of the Hattori Declaration in connection with the "Multipexers vs. Logic Circuits" issues.

> Our law requires patent challengers to prove invalidity by clear and convincing evidence. Where an accused infringer is clearly practicing only that which was in the prior art, and . nothing more, and the patentee's proffered construction reads on the accused device, meeting this burden of proof should not prove difficult. Nevertheless, accused infringers are not free to flout the requirement of proving invalidity by clear and convincing evidence by asserting a "practicing prior art" defense to literal infringement under the less stringent preponderance of the evidence standard.[34]

Defendants had their opportunity to convince the jury that the claims, as construed by the Court, read on the prior art. Apparently they failed in this, for the jury concluded that the claims were not invalid. They cannot now, long after the claims have been construed and their validity has been tried, revisit the same issues under the guise of noninfringement.

Multiplexers vs. Logic Circuits

Claims 16 and 17 recite "A multiplexer circuit comprising" several TGM stages hooked together in a certain way. Despite plaintiff's belated suggestion that this preamble is not a claim limitation (PB-II at 17-18; PB-III at 4),[35] the parties agreed on a

---

[34] Tate Access Floors Inc. v. Interface Arch. Res. Inc., 279 F.3d 1357, 61 USPQ2d 1647, 1654 (Fed. Cir. 2002).

[35] It is somewhat surprising to see plaintiff urging that the term "multiplexer," as construed by the Court, is not a claim

(...continued)

construction of the term multiplexer and the Court adopted it and so instructed the jury: "A circuit that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals." This is much more than a mere statement of purpose or intended use for the claimed invention; it is necessary to give life, meaning, and vitality to the claim, for it describes what the claimed invention is and does.[36] Thus, no accused circuit can be found to literally infringe claims 16 and 17 unless it in fact does what the Court's construction says it must.

As indicated, plaintiff has, by way of the Randolph declarations, made a prima facie showing that each of the accused circuits is a multiplexer circuit within the meaning of that term as construed

---

limitation. As will be seen, it is the presence of that limitation that renders many of defendants' asserted factual issues immaterial, as a matter of law, to the question of literal infringement.

[36] See Catalina Mktg. Int'l Inc. v. Coolsavings.com Inc., 289 F.3d 801, 62 USPQ2d 1781, 1784-85 (Fed. Cir. 2002). As plaintiff admits, "[t]he final output signal is never mentioned in the Claims." (PB-II at 28). Thus, the term "multiplexer" is clearly necessary to give meaning to the claim. Without it, the claimed structure would be simply a serial arrangement of TGM's, hooked up in a certain way, with no particular function. This is borne out by the presence of the "whereby" clauses (not construed as limitations): e.g., "whereby the circuit forms a three-to-one multiplexer."

by the Court. Defendants attack plaintiff's prima facie case on these asserted grounds[37]:

> (1) An accused circuit can be a multiplexer within the meaning of that term as construed by the Court "only if its logic equation is the same as that for a serial multiplexer claimed in claims 16 and 17. * * * None of the accused circuits has a function that is NPN logically equivalent to the function of the 4:1 or 5:1 serial multiplexers of claims 16 and 17. Therefore, none of the accused circuits is a multiplexer." (DB-I at 6-7, 12)
>
> (2) Plaintiff's witnesses have admitted in testimony that logic circuits are not multiplexers and have distinguished prior art on that ground. The accused circuits are logic circuits. Therefore plaintiff should be judicially estopped to contend that the accused circuits are multiplexers. (DB-I at 6, 10-14)
>
> (3) Plaintiff's witnesses have testified that a multiplexer circuit according to claims 16 and 17 permits exchanging inputs without altering the logical function of the overall

---

[37] In actuality, it has been difficult to separate and categorize defendants' various arguments. As plaintiff complains, "they combine and conflate their arguments to create the impression of many slightly different, hard to grasp, interrelated arguments. They need to be clarified to be categorized." (PB-III at 1) Nonetheless, this represents the SM's best effort to make some useful categorization.

circuit. Certain of the accused circuits do not pass this test and plaintiff should accordingly be judicially estopped. (DB-I at 8, 18-19)

(4) Plaintiff's witnesses have testified that a parallel multiplexer may be substituted for the claimed serial multiplexer without altering the logical function of the overall circuit. Certain of the accused circuits do not pass this test and plaintiff should accordingly be judicially estopped. (DB-I at 8, 19-20)

These grounds are addressed in order.

Logic equations and logical equivalence. Defendants' experts suggest that "[o]ne method for determining whether a particular circuit is a multiplexer within the scope of claims 16 or 17 – or a logic circuit outside their reach – is to derive the logic equation for the particular accused circuit. If it is 'NPN equivalent' to the equation for a serial multiplexer as claimed in the '666 patent, then the circuit is a claimed multiplexer; but if not, then the circuit is a logic circuit outside the scope of the claims." (DB-I at 12) These assertions ignore entirely the Court's construction of the term "multiplexer" as a circuit "that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals." Between them, defendants' experts Sechen and Tredennick have submitted approximately 375 pages of excruciatingly detailed reports and declarations in support of defendants' opposition to plaintiff's motion for summary judgment. Nowhere in those pages has the SM found

any assertion that the accused circuits, as schematically depicted in the extractions relied upon by them and by plaintiff's expert Randolph, do not contain structure that performs that function.[38]

Moreover, the '666 patent nowhere proposes an objective test for a multiplexer that contemplates NPN equivalence. If defendants wished to have the Court consider and adopt a claim construction for the term "multiplexer" that incorporated such a test, they should have proposed it during that phase of the litigation. Instead, the parties agreed on the construction adopted by the Court.

Defendants' arguments and evidence about logical equivalence raise factual issues that are not material, as a matter of law, to the question of literal infringement.

Logic circuits vs. multiplexers. In the discussion that follows, it should be kept firmly in mind that the '666 patent itself begins with some very pertinent language: "The present invention relates to the field of digital logic circuits and, in particular, relates to improved multiplexer circuits." Any reader would conclude that the inventor regarded multiplexer circuits as a subset of digital logic circuits and that the patent should be read accordingly. Defendants therefore face an uphill battle in attempting to convince the Court that, because someone concludes that an accused circuit is a "logic circuit," it cannot also qualify as a

---

[38] But see the discussion of the Hattori declaration.

"multiplexer" as that term is used in the patent and in claims 16 and 17.

Obviously the agreed claim construction for the term (a circuit "that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals") does not exclude some broad class of digital circuits known as "logic circuits." For this reason, the opinions of defendants' experts on that subject do not raise issues of fact that are material to literal infringement. Although they go to great lengths to establish that the accused circuits are in fact "logic circuits," that fact is immaterial to whether the circuits are "multiplexers." Defendants' only recourse is to attempt to establish that, by reason of prior inconsistent testimony and argument on that subject, plaintiff should be judicially estopped from contending that the accused circuits (if they be logic circuits, which we must assume they are for purposes of summary judgment) are multiplexers. In other words, defendants are urging that by reason of its prior utterances, plaintiff has admitted the materiality of the "logic circuit vs. multiplexer" issue.

Defendants point to several instances of alleged inconsistency. First, they cite the deposition testimony of Prof. Wilde, where he indicated that not all cascade structures of 2:1 multiplexers form 4:1 multiplexers. (DB-I at 10) This is doubtless a proposition with which nobody involved in this litigation would disagree – 2:1 multiplexers can be cascaded in ways to perform other logical functions. But it appears in no way inconsistent with plaintiff's position that the particular cascaded arrangements

of 2:1 multiplexers present in the accused circuits form 4:1 or 5:1 multiplexers. So too with Mr. Tran's trial testimony. (DB-I at 11) It is clear that he was simply indicating that TGMs can be hooked up to perform logic functions rather than multistage multiplexers. So too with Prof. Wilde's trial testimony (Ibid) and plaintiff's counsel in closing argument (DB-I at 12). What they were saying, clearly, is that TGMs can be used to build logic circuits that can perform various logical functions, one of which is selection or "multiplexing." Far from being clearly inconsistent with plaintiff's present position on infringement, these statements seem perfectly consonant with it: TGMs can be arranged to perform different logical functions, and when they are arranged serially and provided with appropriate input and control signals to perform a 4:1 or 5:1 selection function, they are multiplexers within the meaning of claims 16 and 17 as construed by the Court. Accordingly, these statements can create no judicial estoppel.

Exchanging inputs. Defendants argue that certain of the accused circuit paths do not permit the exchange of input signals without altering the logical function of the circuit. (DB-I at 19) Here again, the agreed construction of "multiplexer" comprehends no such requirement, so defendants are relegated to their judicial estoppel argument. They state that Translogic's expert Wilde "testified that the claimed multiplexer circuits permitted inputs to be exchanged without affecting the operation of the circuit." (DB-I at 18) Defendants' expert Tredennick opines that many of the accused circuit paths do not permit exchange of inputs. (TR-II at 43 & Ex. 4)

Reading Wilde's testimony (DB-I at 18-19) in context reveals that he was identifying one advantage possessed by the claimed multiplexer that was not available in prior art adder circuits: the possibility that input signals could be exchanged. But even if this advantage had been described in the '666 patent specification, it would not become a requirement for infringement unless it were an express limitation of the claims, or unless the specification or prosecution history compelled a claim construction that would effectively make it a limitation. No such construction was adopted in this case. And the fact that defendants, in certain of the accused circuits, chose not to make use of an unclaimed advantage cannot avoid infringement.[39] Consequently, Wilde's testimony is not clearly inconsistent with plaintiff's current position on literal infringement, even if it be true (and that must be assumed for purposes of summary judgment) that certain of the accused circuits do not permit input interchange. Wilde's testimony creates no judicial estoppel.

Substitution of parallel for serial. Defendants' position here is very similar to its position on

---

[39] It is irrelevant whether an element has capabilities in addition to that stated in the claim. Vulcan Eng'g Co. v. FATA Alum. Inc., 278 F.3d 1366, 61 USPQ2d 1545, 1550 (Fed. Cir. 2002). Imperfect practice of an invention does not avoid infringement. Paper Converting Mach. Co. v. Magna-Graphics Corp., 745 F.2d 11, 223 USPQ 591, 597 (Fed. Cir. 1984). Inefficient infringement is infringement still. Shamrock Techs. Inc. v. Medical Sterilization Inc., 903 F.2d 789, 14 USPQ2d 1728, 1731 (Fed. Cir. 1990).

exchanging inputs. They point to the fact that Wilde testified that although the prior art adder circuits showed three TGMs in series, they were not connected to form a series multiplexer because "those three TGMs in series cannot be rearranged in the old-fashioned way of what we call a tree structure, or parallel multiplexer." (DB-I at 20) Again, the agreed construction of "multiplexer" does not incorporate a requirement that such a rearrangement be possible. It is plain that Wilde was simply pointing out that, if such a rearrangement were made in the prior art adder circuits, the adder would not add. In other words, the function of the circuit would be changed. This was in contrast to the claimed multiplexer, where such a rearrangement would still yield a multiplexer function, albeit one that would not infringe. Defendants are not suggesting that Hitachi's chips have incorporated such a rearrangement or substitution, but simply that such a substitution could not be made "without altering the logical function of the circuit." This, of course, is neither here nor there, for such a substitution would result in no infringement. Wilde's testimony is in no way inconsistent with plaintiff's position on literal infringement and creates no judicial estoppel.

The Hattori declaration. This declaration was submitted very late in the game as an accompaniment to defendants' November 1, 2004 brief. As they characterize it there,

> The Hattori Declaration explains why the DO circuit paths identified by Dr. Sechen cannot, as a matter of law, infringe the '666 patent because the final TGM structure accused by Translogic does not operate to select one of two

> inputs, as TGMs are required to do within the meaning of the claims. Consequently, the accused circuits do not operate as N:1 multiplexers because they only are capable of selecting from N minus one signals. (DB-IV at 2-3)

Plaintiff objects to the Hattori declaration as "conclusory, tardy, and immaterial." (PB VI at 18). The SM is willing to add to these objections with the observation that this declaration, coming only at the eleventh hour, after years of litigation and hundreds of pages of briefing and evidence on the infringement issues, is annoying in the extreme. Defendants have made no effort to show why the facts alleged in the Hattori declaration could not have been brought out much earlier, with a potential saving of much effort and money.

But annoyance is no ground for summary judgment. Plaintiff has pointed to no order of the Court that would preclude defendants from attempting to inject additional evidence of noninfringement, even at this late date. Thus, plaintiff's tardiness objection appears to be unavailing. The allegations in the Hattori declaration must therefore be evaluated for adequacy and materiality. And, of course, the allegations, if competent, must be believed.[40]

---

[40] This, of course, is true only insofar as defendants are the party opposing the motion for summary judgment. By contrast, in considering whether to grant summary judgment in *defendants'* favor on the DO type circuits, it is *plaintiff's* evidence that must be believed. As already indicated, plaintiffs

(...continued)

At the outset, it is important to put this issue in perspective. Mr. Hattori claims that the DO circuit paths do not infringe because the last TGM in the path is configured, before shipment to the United States, so that it is not operational as a TGM. The DO type circuit paths are all contained in a single Hitachi microprocessor, the SH7727. (Exhibit B to DB-II) But circuit paths 1 and 53 in the SH7727 are not asserted by defendants' expert Sechen to be of the DO type. (Exhibit B to DB-II) In addition, circuit paths 10, 14, 54, and 55 appear to have four stages rather than three. In these paths, even if the fourth stage were configured according to Hattori's allegation, claim 16 (which requires only three stages), would still be in play. Accordingly, even if the allegations in the Hattori declaration were ultimately successful in avoiding a finding of infringement as to the other paths in the SH7727, that product would still be at risk with regard to six of its paths: 1, 10, 14, and 53-55.

Hattori's competence with respect to the allegations in his declaration seems clear enough. Although he does not, as pointed out by plaintiff (PB-VI at 19), have any first hand knowledge of what SH7727 customers in the United States know and

---

expert Randolph reviewed all the accused circuits and concluded, among other things, that the various stages each included a TGM that operated as a 2:1 multiplexer. Accordingly, despite Hattori's contrary conclusion, at least that genuine issue of fact would remain for trial. In the event a trial is ordered on the DO circuits, it is recommended that plaintiff be permitted sufficient discovery to test the allegations of the Hattori declaration. See Rule 56(f), FRCP.

do, he is certainly in a position to know what Hitachi does in connection with that microprocessor before shipping it. If it is true (and that must be accepted for purposes of defendants' opposition to plaintiff's summary judgment motion), as he says, that the circuit paths in question are configured prior to shipment to "apply a fixed voltage to the select line of the TGM structure," then the inquiry becomes one of materiality. In other words, does a disabling "configuration" prior to entry into the United States result in a noninfringing product in the hands of a U.S. customer?

The answer to this question is not as clear as one would like. There is no intent element to direct infringement. If a device is capable of being operated in an infringing mode, it need not be shown that customers were told how to do it, or even that they were told it was possible.[41] But a device does not infringe simply because it is possible to alter it in a way that would satisfy all the limitations of a patent claim.[42] The Federal Circuit has not articulated a bright-line test for determining whether a capability

---

[41] See Intel Corp. v. United States ITC, 946 F.2d 821, 20 USPQ2d 1161, 1171 (Fed. Cir. 1991).

[42] E.g., High Tech Med. Instr. Inc. v. New Image Indus. Inc., 49 F.3d 1551, 33 USPQ2d 2005, 2008 (Fed. Cir. 1995). "[T]hat a device is capable of being modified to operate in an infringing manner is not sufficient, by itself, to support a finding of infringement." Telemac Cellular Corp. v. Topp Telecom Inc., 247 F.3d 1316, 58 USPQ2d 1545, 1554 (Fed. Cir. 2001). Compare Bionx Implants Inc. v. Linvatec Corp., 299 F.3d 1378, 64 USPQ2d 1145, 1148 (Fed. Cir. 2002).

of infringement amounts to infringement. Instead, it has suggested that the answer depends on what the device "was intended to do and did do."[43] Thus, as can be seen, the Federal Circuit has injected a good deal of uncertainty into the inquiry: viz, is intent material or not?

On balance, however, it is clear that this controversy cannot be resolved on summary judgment. Determining the materiality of the pre-shipment reconfiguration itself raises material factual issues about, at the very least, what the device "was intended to do and did do." These issues can only be resolved by trial.

Logically Independent Input and Control Signals

Defendants' basic position here is this: "Second, many of the accused circuits do not have the requisite number of independent 'input variables,' as the claims require. Third, other of the accused circuits have input signals and control signals that are logically dependent or control signals logically dependent on one another. Translogic has admitted that such dependencies cannot occur within a claimed multiplexer." (DB-I at 9)

---

[43] High Tech, supra note 42. The court denied that Intel (supra note 41) stands for the proposition that if a particular device can be altered without undue difficulty to operate in an infringing manner, the device, as sold, must be deemed to infringe.

Defendants' experts, who must be believed at this stage, say that many of the accused circuits do not infringe because, owing to connections through surrounding circuitry, there are dependencies among inputs and control signals. "These dependencies might be between two input signals, between two control signals, or between an input signal and a control signal. There may be multiple dependencies among inputs and control signals." (E.g., TR-II ¶135) They also say that some accused circuits "have an input that is connected to the output through a latch so that it cannot be an independent input variable, but instead always is the previous output value." (Ibid) Plaintiff responds that signal dependencies established through surrounding circuitry are not material to the question of literal infringement, because the claims, as construed by the Court, do not require independence among the various signals, only that there be 4 input variables and 3 control signals (claim 16) or 5 input variables and 4 control signals (claim 17). Plaintiff is willing to concede that no two of these input variables and control signals may be a common single signal that is "coupled" to two input or control terminals. The construction of "coupled" adopted by the Court was "connected to, directly or through one or more intervening inverters or buffers." So plaintiff's position is that, so long as a single signal is not connected, directly or through an inverter or buffer, to more than one input or control terminal, the fact that two signals may be found to have, after tracing through surrounding circuitry, a common origin is immaterial.

Plaintiff is correct. Contrary to defendants' repeated assertions, the claims do not contain a

limitation that the signals be "independent." It is clear from the context of the claims as a whole that they cannot all be the same directly coupled signal; the claimed circuit would not perform a multiplexer function under such circumstances. But the claim language does not preclude a common source for two or more signals that, after traversing surrounding circuitry (sometimes in long paths and sometimes in short paths), are ultimately coupled to two or more input or control terminals of the multiplexer circuit. Similarly, as plaintiff points out, the claims say nothing about the final output of the multiplexer, and therefore do not preclude its use, again after traversing surrounding circuitry, as an input variable or control signal in the multiplexer.

Defendants contend that, with respect to input variables, the Court's claim construction supports their position, because it required that "each must be capable of assuming, at any given time, either one of at least two values." But as plaintiff points out, this construction was based upon the premise that input terminals could not be permanently tied to voltage or ground. As the SM recommended, the "Court might, for the sake of clarity, wish to instruct the jury further, that this construction means that none of the four or five signal input terminals can be permanently fixed to ground or voltage." (Report I at 44) Defendants respond that "[t]he Court declined to give to the jury the proposed further instruction from the original Claim Construction Report. That additional language cannot now be used to modify the words of the definition as given." (DB-IV at 8) Plaintiff counters by pointing to the Court's Order of October 6, 2003 (Exhibit 1 to PB-VI), which clearly

states: "The special master's first and second reports and recommendations * * * are adopted."

Defendants' position on this point is simply wrong. In the first place, it supposes that the SM was proposing the two definitions as *mutually exclusive alternatives*. Nothing could be further from the truth. The SM was suggesting that, if it appeared to the Court at instruction rendering time that the jury might not fully understand what was meant by "at any given time," the Court would be able to clarify that meaning by indicating that it precluded tying terminals permanently to voltage or ground. The fact that the jury was not given the additional clarifying instruction does not indicate, at least to the SM, that the Court was *rejecting the very basis given by the SM for the instruction in the first place*. Indeed, the express adoption of the SM's claim construction reports demonstrates just the opposite conclusion – that the Court had adopted the SM's reasoning and recommendations and would appropriately instruct the jury, as necessary, in a manner consistent with those recommendations. And that is precisely what happened at the validity trial. Obviously no issue came up that, in the view of the Court, made it likely that the jury would be confused by the term "at any given time." Thus, the clarifying instruction was not needed. And just as obviously, the fact that the clarifying instruction was not given at the validity trial does not compel the SM

to ignore it now, and in so doing alter the very basis for construction of the term "input variable."[44]

Defendants observe that the SM's claim construction reports "were neither admitted into evidence nor provided to the jury in the validity trial" and hint darkly that, if they had been, "the result of the validity trial might well have been quite different." (DB IV at 5) But they never do show how, if the suggested clarifying instruction had been given, it would have had any impact on the outcome.[45] Finally, they fall back on the axiom that claims must be construed in the same way for infringement as for validity. (DB-IV at 9) But that is exactly what is happening here. The SM is using the definition of "input variable" recommended by him and adopted by the Court: an input variable must be capable of assuming *either one* of at least two values at any given time; this precludes tying the input permanently to voltage or ground. But it does not require that the signal be capable of assuming *both* of the two values at any given time, and therefore does not preclude, as urged by defendants, the value of one input signal being predetermined by another input signal through surrounding circuitry. (DB-I at

---

[44] In other words, defendants want the SM to disregard the underlying basis for the definition of "input variable," which is that is could not be always high or low, or always 1 or 0, or always voltage or ground.

[45] The best they come up with is two examples of other possible clarifying instructions that were not given and therefore allegedly permitted plaintiff to make contrary arguments at the validity trial. (DB-IV at 9)

15) At another "given time" the value of the latter could change, thus changing the value of the former.

Accordingly, here again defendants can prevail only by establishing an equitable case for judicial estoppel, based upon testimony or representations in prior proceedings. In attempting to do this, they point to three sources: three lines from plaintiff's opening statement at trial (DB-I at 14), certain testimony of Wilde (Id. at 15-17), and plaintiff's appeal brief in the reexamination proceeding.

The opening statement was simply to the effect that, in the invention described in claim 16, the seven signals coming in are logically independent. This statement does not appear to be clearly inconsistent with plaintiff's current position that surrounding circuitry is immaterial. To the contrary, it is clearly consistent with plaintiff's concession that no two incoming signals can be directly coupled from a common source. The same is true with the Wilde testimony cited by defendants. Read in context, it simply reflects his opinion that, because the prior art circuits in question had inputs or control signals directly coupled from a common source, they did not produce a multiplexer function. Far from being inconsistent with plaintiff's position on literal infringement, this testimony is perfectly consistent. Neither the opening statement nor the Wilde testimony creates a judicial estoppel.

With respect to the appeal brief, defendants point out that it contains statements that the input variables and control signals must be "different," and conclude that "different" is equivalent to "independent" in this context. (DB-IV at 15) They

follow by arguing that plaintiff thereby "expressly disclaimed * * * any application of claims 16 to circuits that do not have four (or five) different, *independent* input variables and three (or four) different, *independent* control signals." (DB-IV at 18; emphasis added) The SM disagrees. Reading the statements as a whole, it is not possible to come away with a conviction that plaintiff was expressly disclaiming possible signal dependence.[46]

More Than One TGM Per Stage

The claims call for first, second, third (claim 16), and fourth (claim 17) "stage TGM circuit[s]." During the claim construction phase, the SM concluded that the term "stage" needed no construction and could even be disregarded, so that the claims could be viewed as calling for first, second, third, and fourth TGM circuits. Nonetheless, the parties were in agreement that a "stage" has only a

---

[46] Defendants argue that the discussion of the Tosser reference in the brief establishes that plaintiff was equating "different" with "independent." (DB-IV at 15) But this is not of all clear from the quoted portions of the brief. What plaintiff was arguing was that Tosser did not show "different" input variables. What was clear was that plaintiff did not regard a signal and its complement as "different." And plaintiff concedes, as indicated above (see p. 25) that a signal that is merely passed through an inverter is not different from its original. But this is a far cry from conceding that signals that are processed through more complex logic circuitry, such as NAND, NOR, and XNOR gates and Flip-Flops, are not different, or that the claims exclude signals that have a common original source.

single TGM circuit, so it was suggested that the jury might be so instructed. (Report I at 38-39)

Defendants' experts have concluded that, in certain circuit paths (at least those identified in Ex. B to DB-II as "Circuit Path Type Parallel"), some of the stages have more than one TGM. (TR-II ¶136; SR-II ¶¶324-30) It should be noted that their consequent conclusions of noninfringement are based in part on the similarity of those circuits to prior art circuits. As indicated above in the Tredennick Summary discussion, prior art plays no role in the determination of literal infringement. Nonetheless, the experts raise a genuine issue as to whether those particular accused paths do in fact have stages that include more than one TGM circuit. That factual issue is material because an accused circuit cannot, as a matter of law (established by the earlier proceedings in this litigation), literally infringe if one or more of its stages includes more than one TGM circuit. Although plaintiff contests the factual issues (E.g. RD-II at 9), defendants' experts must, for purposes of this motion, be believed. This issue remains for trial.

Unfortunately, in the briefing directed at the SM's proposed report, defendants injected a controversy as to which circuit paths properly belong in the "Parallel" category. In his restated declaration (TD-II), their expert Tredennick had constructed a table (Exhibit 4) that corresponded to Exhibit B to DB-II with respect to the circuit paths grouped in the

"Parallel" category.[47] Attached to his supplemental declaration, however, was an "updated" Exhibit 4, which he explained only as follows:

> In view of additional work undertaken by Dr. Sechen, as set forth in [SR-II], and my own further analysis *as set forth herein*, I have updated Exhibit 4 to my Supplemental and Restated Expert Disclosure Statement. (TD-III ¶12; emphasis added.)

There are several problems with this explanation. First, Tredennick does not discuss, in TD-III, the "Parallel" path category, which seems clearly inconsistent with the italicized words above. Nor does he inform the reader that he has added several paths to that category in addition to those identified by Sechen in Exhibit B, much less, say which ones. Nor do defendants in their brief. All they say is:

> Of particular note, Exhibit 4 now shows some additional circuit paths that should properly be included in the "parallel" category type for reasons explained in the Tredennick Restated Report. *See* Tredennick Restated Report at ¶110. (DB-IV at 2)

---

[47] The circuit paths identified in Exhibit 4 as having more than one TGM per stage were those categorized as "Parallel" type in Exhibit B to DB-II (with the exception of SH7294 Path 24, which appeared in Exhibit 4 but not Exhibit B, a discrepancy which remains unexplained but is surely of no significance in the end).

As a consequence, the SM found it necessary to painstakingly compare Updated Exhibit 4 with both Exhibit 4 and Exhibit B in order to ascertain which circuit paths Tredennick had added to Updated Exhibit 4. These turned out to be Paths 2-7 in nine products identified as SH7750, SH7750R, SH7750S, SH7751, SH7751R, SH7760, SH7901, SH7901R, and SH7091T.

Thus, Tredennick really does not offer any explanation whatever for his belated inclusion of these additional circuit paths in the "Parallel" category. Defendants say that the explanation can be found at ¶110 of his restated report. The SM has reviewed that paragraph, but it does not appear to address the "one TGM per stage" issue. Certainly it does not do so in any direct manner; rather, it appears to deal with shared control lines, another issue altogether.

A party opposing summary judgment must show an evidentiary conflict on the record; mere denials or conclusory statements are not sufficient.[48] As indicated previously, plaintiff's expert Randolph conducted a detailed analysis sufficient to establish a prima facie case of literal infringement by all the accused circuit paths. Also as indicated, defendants' experts have sufficiently countered that showing with respect to the "Parallel" type circuit paths identified in Exhibit B to DB-II, by demonstrating a genuine issue of material fact as to whether those

---

[48] E.g., Interpart Corp. v. Italia, 777 F.2d 678, 228 USPQ 124,126 (Fed. Cir. 1985).

paths include more than one TGM per stage. But ¶110 of Tredennick's restated report does not begin to counter that showing with respect to the additional paths identified in Updated Exhibit 4. In the end, Updated Exhibit 4 is, with respect to those additional the very epitome of a mere denial or conclusory statement that does not point to an evidentiary conflict. Accordingly, it is recommended that the trial with respect to the "one TGM per stage" literal infringement issues be limited to the circuit paths identified as belonging to the "Parallel" category in Exhibit B to DB-II.

Reverse Doctrine of Equivalents

In its classical 1950 decision on the doctrine of equivalents, Graver Tank, the Supreme Court assured that:

> In determining whether an accused device or composition infringes a valid patent, resort must be had in the first instance to the words of the claim. If accused matter falls clearly within the claim, infringement is made out and that is the end of it.

But is that *really* "the end of it?" The Court went on to observe that the:

> wholesome realism of [the doctrine of equivalents] is not always applied in favor of a patentee but is sometimes used against him. Thus, where a device is so far changed in principle from a patented article that it performs the same or a similar function in a substantially different way, but nevertheless falls within the literal words of the claim, the

> doctrine of equivalents may be used to restrict the claim and defeat the patentee's action for infringement.[49]

Under the Federal Circuit's modern formulation of this so-called "reverse doctrine equivalents," an accused product or process that falls within the literal words of a claim nevertheless may not infringe if the product or process is so far changed in principle from a patented article that it performs the same or a similar function in a substantially different way. The doctrine is equitably applied based upon underlying questions of fact, when the accused infringer proves that, despite the asserted claims literally reading on the accused device, "it has been so changed that it is no longer the same invention."[50] Reverse equivalents is not a part of the literal infringement termination; rather, it is a

---

[49] Graver Tank & Mfg. Co. v. Linde Air Prods. Co., 339 U.S. 605, 607-09, 85 USPQ 328 (1950).

[50] E.g., Amgen Inc. v. Hoechst Marion Roussel Inc., 314 F.3d 1313, 65 USPQ2d 1385, 1413 (Fed. Cir. 2003). Just as the purpose of the doctrine of equivalents is to prevent pirating of the patentee's invention, so the purpose of the reverse doctrine of equivalents is to prevent unwarranted extension of the claims beyond a fair scope of the patentee's invention. The issues raised by new technologies require considered analysis. Scripps Clinic & Res. Found v. Genentech, Inc., 927 F.2d 1565, 18 USPQ2d 1001, 1013-14 (Fed. Cir. 1991).

defense that can defeat liability where literal infringement has been established.[51]

Thus, if the patentee makes a showing (as plaintiff has done here with respect to most of the accused circuits) that the claim words read literally on the accused matter, the accused infringer may undertake the burden of going forward to establish the fact of noninfringement under the reverse doctrine of equivalents. If the accused infringer makes a prima facie case, the patentee, who retains the burden of persuasion on infringement, must rebut that prima facie case.[52]

In their main brief, defendants urge that they have discharged their burden of going forward under the reverse doctrine of equivalents in two major respects. (DB-I at 26) First, they assert that the accused circuits "are entirely changed in principle from the simple multiplexers that are the subject of claims 16 and 17"; this because they do not have the same logical function as the claimed multiplexers. Second, they assert that the accused circuits "perform in substantially different ways from the multiplexers of claims 16 and 17"; this because the control and input signals are not logically independent. As indicated above, the SM has concluded, as a matter of law, that these assertions

---

[51] See Martin v. Barber, 755 F.2d 1564, 225 USPQ 233, 234 n.1 (Fed. Cir. 1985) (The doctrine "becomes an issue only when the accused device falls within the literal words of the claim.").

[52] SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 227 USPQ 577, 587 (Fed. Cir. 1985).

about logical function and logical independence are not material to the question of literal infringement. That is not to say, however, that such assertions might not have relevance to the factual questions raised by the reverse doctrine of equivalents. It is clear to the SM that the factual assertions by defendants' experts raise genuine issues of material fact that would preclude a summary judgment rejecting that defense, if defendants are entitled as a matter of law to assert the defense. Plaintiff says they are not.

Plaintiff denies applicability of the reverse doctrine of equivalents, on three basic grounds. First, it suggests that the Federal Circuit has repudiated the doctrine. (PB-II at 4) Second, it attacks defendants' prima facie showing of reverse equivalents, largely on the basis of the trial testimony of defendants' expert Sechen. (PB-V at 5-10) Finally, it says that, in any event, defendants "did not plead that defense, and so have waived it." (PB-II at 5; PB-V at 4, 20)

Plaintiff cites no authority for this latter proposition. The only Federal Circuit cases touching on the matter that the SM has been able to find both deal with a failure to make arguments below, not a failure to plead.[53] The SM has found no lower court precedent on point. It is true that "[o]ne does not make a reverse doctrine of equivalents argument

---

[53] Texas Instr. Inc. v. United States ITC, 988 F.2d 1165, 26 USPQ2d 1018, 1027 (Fed. Cir. 1993); Rolls-Royce Ltd. v. GTE Valeron Corp., 800 F.2d 1101, 231 USPQ 185,190 (Fed. Cir. 1986).

simply by mounting a defense to literal or doctrine of equivalents infringement,"[54] but this is because after a case of literal infringement has been made out, the burden shifts to the accused infringer to come forward with evidence supporting a reverse doctrine of equivalents defense. It would be a long stretch to conclude that a pleading denying literal infringement does not fairly subsume such a defense. In the absence of compelling authority to the contrary, defendants should be permitted to assert the defense in response to plaintiff's motion for summary judgment of infringement.

Plaintiff's first objection presents a more difficult question. It refers to the 2002 decision in Tate v. Interface, where a panel of the Federal Circuit observed that "[n]ot once has this court affirmed a decision finding noninfringement based on the reverse doctrine of equivalents." [55] The SM has in his own work viewed this decision as having "rather pointedly cast doubt on the continuing vitality of the reverse doctrine of equivalents."[56] Plaintiff goes further, and says that "the Federal Circuit has recently held that there is no 'reverse doctrine of equivalents' defense," citing Tate v. Interface. (PB-II at 4) This goes too far, for several reasons.

---

[54] Texas Instr., supra note 53.

[55] Tate Access Floors Inc. v. Interface Arch. Res. Inc., 279 F.3d 1357,61 USPQ2d 1647,1655 (Fed. Cir. 2002).

[56] Robert L. Harmon, Patents and the Federal Circuit 346 (6th ed. 2003).

First, Graver Tank has never been overruled and, indeed, was expressly reaffirmed by the Supreme Court in its 1997 Warner-Jenkinson decision.[57] Thus, any panel of the Federal Circuit would be obligated to follow Graver Tank and, for that matter, the Federal Circuit's own prior precedent on the subject of reverse equivalents.[58] Second, the notion that the Patent Act of 1952 was intended to have any impact upon Graver Tank was specifically rejected in Warner-Jenkinson.[59] Indeed, the Federal Circuit has itself recognized that though the enactment of 35 U.S.C. §112¶6 may not have been intended to codify the reverse doctrine of equivalents, it may have had that *result*.[60]

Finally, the statements in Tate v. Interface are more properly viewed as dictum. As already noted in connection with the Tredennick Summary, the accused infringer there, not unlike defendants

---

[57] Warner-Jenkinson Co. v. Hilton Davis Chem. Co., 520 U.S. 17, 41 USPQ2d 1865, 1870-71 (1997).

[58] Decisions of a three-judge panel cannot overturn prior precedential decisions of the court. Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). A reversal of such a holding would have to be through an en banc proceeding in the Federal Circuit, Supreme Court review, or a change in the patent statute by Congress. Jacobs Wind Elec. Co. v. Florida Dep't. of Transp., 919 F.2d 726, 16 USPQ2d 1972,1973-74 (Fed. Cir. 1990).

[59] Warner-Jenkinson Co. v. Hilton Davis Chew. Co., 520 U.S. 17,41 USPQ2d 1865,1870-71(1997).

[60] In re Donaldson, 16 F.3d 1189, 29 USPQ2d 1845, 1849 & n. 5 (Fed. Cir. 1994).

here, was arguing that it could not be held to infringe because it was, in effect, merely "practicing the prior art." It cited the reverse doctrine of equivalents as exemplary of another circumstance which may result in a finding of noninfringement even when the accused device possesses each and every limitation of an asserted claim. In rejecting the possibility of an affirmative defense based on "practicing prior art," the Tate v. Interface panel also rejected the accused infringer's reverse equivalents analogy, declaring that "[e]ven were this court likely ever to affirm a defense to literal infringement based on the reverse doctrine of equivalents, the presence of one anachronistic exception, long mentioned but rarely applied, is hardly reason to create another. This is strong language, no doubt. But it falls well short of wholesale abandonment of reverse equivalents as a defense to literal infringement.

On the basis of the foregoing, the SM would be loath to recommend that the Court in this case pronounce the death knell of the reverse doctrine of equivalents, as urged by plaintiff. Unless and until the doctrine is expressly abandoned by a higher court, an accused infringer faced with a finding of literal infringement should be permitted to attempt to prove that the accused device is so far changed in principle from the claimed device that it performs the same or a similar function in a substantially different way or that it has been so changed that it is no longer the same invention, and thereby avoid liability for infringement.

Plaintiff also appears to argue that the reverse doctrine of equivalents, like the traditional doctrine of equivalents,[61] requires an element-by-element approach. It cites no authority for this proposition, and the SM is aware of none. Indeed, the closest Federal Circuit authority would seem to point in the opposite direction.[62] Moreover, as defendants cogently point out, plaintiff's argument "makes no sense whatsoever, since by definition the doctrine cannot apply until all elements of the claim are literally present." (DB-V at 1) In other words, the element-by-element analysis has already been made, and resolved in plaintiff's favor; now the focus shifts to the extent to which the accused circuits are changed in principle from the claimed circuits.

Defendants say they can demonstrate that the accused circuit paths, when considered in connection with surrounding circuitry, are so far changed in principle from the circuits of claims 16 and 17 that they perform the same or a similar function in a substantially different way or that they have been so changed that they are no longer the same invention. Defendants offer an impressive array of expert opinion in support of their contention. Plaintiff has offered equally impressive expert opinion to the

---

[61] See, e.g., Cooper Cameron Corp. v. Kvaerner Oilfield Prods, Inc., 291 F.3d 1317, 62 USPQ2d 1846, 1849-50 (Fed. Cir. 2002).

[62] In United States Steel Corp. v. Phillips Petroleum Co., 865 F.2d 1247, 9 USPQ2d 1461, 1466 n.9 (Fed. Cir. 1989), the court approved the district court's use of a test for reverse equivalents that focused on the "principle" of the contribution made by the inventor.

contrary. Plaintiff's contention regarding the alleged inconsistency of Sechen's testimony is no more pertinent to reverse equivalents than was the testimony of Tran and Wilde pertinent to plaintiff's prima facie showing of literal infringement. In neither situation was the context sufficiently analogous to warrant a conclusion that the prior testimony was clearly inconsistent with the party's current position. In no instance were the witnesses testifying about the accused circuit paths.

The conflicting opinions raise genuine issues of fact about the possible differences between the accused and claimed circuits, and the significance of those differences. Those issues of fact are, as a matter of law, material to the reverse equivalents defense interposed by defendants. Obviously, those issues of fact cannot be resolved on motion for summary judgment. They must be tried, either by a jury, or by the Court in the event both parties are willing to waive jury trial.

The matter of selection of representative circuits needs to be addressed at this point. First it is necessary to examine the real heart of the controversy. Although the parties made their proposals for selection of representative circuits with literal infringement in mind, the selection process is at least as important and at least as difficult in connection with the reverse equivalents defense. Basically, plaintiff contends that the circuitry surrounding the accused circuit paths is irrelevant. Defendants' disagree, contending that to be "the essential factual issue of the case." (DB-I at 21) As we have seen, plaintiff's view prevails with respect to literal infringement, because defendants' factual

assertions about the impact of the surrounding circuitry on the accused paths are not material a matter of law to the question of literal infringement (except in the case of the circuits that defendants assert have more than one TGM per stage). But defendants' assertions are most assuredly material to the defense of reverse equivalents, thus presenting essentially the same set of selection problems.

The basic idea here, of course, is to save the parties and the Court the burden and expense of separately analyzing 344 circuits. Some short cuts ought to be possible. Hence the proposal for selection of representative circuits, so that a decision as to one such circuit will apply, without further analysis, to all circuits of which it is representative. The fly in this soothing ointment is the surrounding circuitry issue. Plaintiff felt with respect to literal infringement (and will undoubtedly feel the same with respect to reverse equivalents) that the longer and more complex the "loop" through surrounding circuitry, the easier it would be to establish infringement. Defendants of course prefer the shortest possible loops. These are perfectly rational and legitimate positions, but they impede the circuit selection process. The problem is exacerbated by the reality that plaintiff bears the burden of proof of liability for infringement. Accordingly, no perfectly safe selection of representatives is possible without defendants' agreement. Defendants could, if they wished, put plaintiff to its proof on all 344 accused circuits, *consistent, of course, with a litigant's obligation to refrain from unduly multiplying proceedings.*

Defendants have offered several proposed categories of circuits. While the categories seem reasonable, they have lumped long-loop and short-loop paths together in each category. Plaintiff complains that, in each instance, defendants have chosen the perceived best example for them – the short loop – as representative of the circuits in a category, which would preclude plaintiff from taking advantage of its perceived best case – the long loop. Defendants are likewise unwilling to accept a long-loop representative that would preclude their short-loop advantage.

The SM's proposed solution to this stalemate is as follows: Using the categories proposed by defendants (see DB-II), let each side select one circuit from each category as representative. If at trial one party prevails on both circuits from a given category, that will of course resolve the entire category. But if the fact-finder should conclude (which the SM personally believes to be unlikely) that one circuit escapes under the reverse doctrine of equivalents while the other does not, further processing may be necessary in order to draw a line somewhere in the loop-length spectrum. This could be done in several different ways. The most efficient procedure would likely be for the Court to appoint an independent technical expert to attempt to draw the line, possibly in connection with the trial of the damages issues.[63] Alternatively, the Court could

---

[63] This could even be done in connection with the reverse equivalents trial; the expert could hear the evidence and then, after a verdict is in, immediately advise the Court as to the appropriate dividing line in the event of a split verdict on one or

(...continued)

appoint this or another special master to revisit the question if that becomes necessary; after the reverse equivalents trial a special master would have a much clearer basis upon which to make recommendations on where the line should be drawn. At the present time, however, there is no rational basis for line-drawing, without substantial expert testimony.[64] Indeed, the line-drawing exercise would, at this point in the proceedings, be inappropriate, for it would require resolution of genuine issues of fact material to the defense of reverse equivalents.

RECOMMENDATIONS

On the basis of the foregoing discussion, it is recommended that the Court make the following rulings with respect to plaintiff's motion for summary judgment of infringement:

> (1) There are no genuine issues of fact that are material to whether the accused circuits are "multiplexer" circuits within the meaning of that term as previously construed by the Court. The factual issues raised by defendants are not material as a matter of law. All of the accused circuits are

---

more categories. The Court could then make a finding and fashion a judgment accordingly.

[64] Any of these approaches will necessarily result, of course, in allocating part of the fact-finding away from the jury and to the Court in the event of a split jury verdict on one or more categories. It would surprise the SM however, to learn that the parties would be unwilling to waive jury trial to that limited extent, in view of the potential savings in time and money.

"multiplexer" circuits within the meaning of that term as construed, and therefore satisfy that limitation of claims 16 and 17.

(2) There are no genuine issues of fact that are material to whether the accused circuits employ "input variables" and "control signals" within the meaning of those terms as previously construed by the Court. The factual issues raised by defendants are not material as a matter of law. All of the accused circuits employ the "input variables" and "control signals" within the meaning of those terms as construed, and therefore satisfy those limitations in either claim 16 or claim 17.

(3) There are genuine issues of fact material to whether certain of the accused circuits (those identified as "Circuit Path Type Parallel" in DB-II Ex. B) meet the limitation of "stage" as previously construed by the Court. If, as a matter of fact, the "stages" of those circuit paths contain more than "a single TGM circuit," they do not literally infringe claims 16 and 17. That factual determination remains for trial by a jury, or by the Court if the parties waive jury trial. At trial, two representative circuits should suffice: SH7190 Path 20, and one to be selected by plaintiff.

(4) Genuine issues of material fact also remain with respect to SH7727 Paths 2-9, 11-13, 15-52, and 56-58. If, as a matter of fact, the final stage in those circuit paths has been configured, prior to entry into the United States, so that it does not operate as a TGM, and if purchasers or users were not intended to and did not or could not actually reconfigure it to operate as a TGM, then those paths

do not literally infringe claims 16 and 17. At trial, two representative circuits should suffice: SH7727 Path 2, and one to be selected by plaintiff.

(5) With the exception of the circuits identified in (3) and (4) above, all of the accused circuits meet all of the limitations of either claim 16 or claim 17 and therefore literally infringe.

(6) There are genuine issues of fact material to defendants' defense of reverse equivalents. Those issues have to do with whether, in defendants' own words, the accused circuits "are entirely changed in principle from the simple multiplexers that are the subject of claims 16 and 17" and "perform in substantially different ways from the multiplexers of claims 16 and 17." Those factual determinations remain for trial by a jury, or by the Court if the parties waive jury trial. If the trial is to a jury, the parties should be admonished that the trial is not about whether the accused circuits meet or fail to meet one or more of the claim limitations as construed by the Court; with the exception of the circuits identified in (3) and (4) above, that determination has already been made in plaintiff's favor. Rather, the inquiry must be directed to whether, and to what extent, the "principle" of the accused circuits differs from that of the claimed circuits.[65] The reverse equivalents defense is asserted for all of the accused circuits. It is recommended that trial be limited to

---

[65] See United States Steel Corp. v. Phillips Petroleum Co., 865 F.2d 1247, 9 USPQ2d 1461, 1466 & n.9 (Fed. Cir. 1989).

representative circuits selected by the parties in accordance with the procedure outlined above in the discussion of reverse equivalents.

Respectfully submitted,

Robert L. Harmon

Special Master

APPENDIX H

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	CV 99-407-PA
v.	)	
	)	OPINION AND ORDER
HITACHI, LTD.,	)	
Defendant.	)	

JEFFREY STEWART LOVE
Klarquist Sparkman, LLP
One World Trade Center
121 SW Salmon Street
Suite 1600
Portland, OR 97204-2988

Attorneys for Plaintiff

DAVID W. AXELROD
Schwabe Williamson & Wyatt
1211 SW Fifth Avenue
suite 1600-1800
Portland, OR 97204-3795

Attorneys for Defendant

PANNER, J.

Plaintiff Translogic Technology, Inc. brings this action for patent infringement against defendants Hitachi Ltd., Hitachi America, Ltd., and Renesas Technology America, Inc. Plaintiff contends that defendants' microprocessors infringe plaintiff's U.S. Patent No. 5,162,666 (the '666 Patent), which is for a "Transmission Gate Series Multiplexer." After the trial on validity, the jury found that claims 16 and 17 of the '666 Patent were neither anticipated nor obvious.

Defendants move for a new trial and for judgment as a matter of law. I deny defendants' motions and conclude that claims 16 and 17 of the '666 Patent are not obvious.

DISCUSSION

The Federal Circuit has jurisdiction over any appeals, and it applies its own law to patent issues. On procedural issues, however, the Federal Circuit defers to regional circuits, so Ninth Circuit legal standards govern defendants' post-trial motions. Shockley v. Arcan, Inc., 248 F.3d 1349, 1358 (Fed. Cir. 2001).

DEFENDANTS' MOTIONS FOR JUDGMENT AS A MATTER OF LAW

I. Standards for Judgment as a Matter of Law

In analyzing a motion for judgment as a matter of law, the court must view the evidence in the light most favorable to the nonmoving party, and must draw all reasonable inferences in favor of that party. Horphag Research, Ltd. v. Pellegrini, 337 F.3d 1036, 1040 (9th Cir. 2003), cert. denied, 72 U.S.L.W. 3393, 3444, 3447 (U.S. Jan. 12, 2004) (No. 03-773). To grant a motion for judgment as a matter of law, the court must find "no legally sufficient evidentiary basis for a reasonable jury to find" in favor of the nonmoving party. Fed. R. Civ. P. 50(a)(1).

"Judgment as a matter of law is proper when the evidence permits only one reasonable conclusion and the conclusion is contrary to that reached by the jury." Ostad v. Oregon Health Sciences Univ., 327 F.3d 876, 881 (9th Cir. 2003). The court may not substitute its view of the evidence for that of the jury. Costa v. Desert Palace, Inc., 299 F. 3d 838, 859 (9th Cir. 2002) (en banc) aff'd, 539 U.S. 90 (2003). The court is not permitted to make credibility determinations or to weigh the evidence. Id.

II. Motion for Judgment as a Matter of Law on Anticipation

A. Standards for Anticipation

An invention is not patentable if it "was known or used by others in this country, or patented or described in a printed publication in this or a

foreign country, before the invention thereof by the applicant for patent, or... was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(a) & (b). "An 'anticipating' reference must describe all of the elements and limitations of the claim in a single reference, and enable one of skill in the field of the invention to make and use the claimed invention." Merck & Co., Inc. v. Teva Pharmaceuticals USA, Inc., 347 F.3d 1367, 1372 (Fed. Cir. 2003). "Anticipation is a question of fact." Medichem, S.A. v. Rolabo, S.L., 353 F.3d 928, 935 (Fed. Cir. 2003).

B. Discussion

Defendants contend that as a matter of law, five items of prior art anticipated claims 16 and 17 of the '666 Patent: the Oklobdzija article; Japan Patent No. 531 (JP '531); JP '529; the Goto article; and the Gorai article.[1] Defendants contend that each of these items of prior art discloses circuits that are structurally identical to the 4:1 and 5:1 serial multiplexers disclosed in claims 16 and 17 of the '666 Patent. Plaintiff responds that the items of prior art cited by defendants are adder circuits or digital logic circuits, rather than multiplexers that select one output from four or five separate inputs.

Defendants argue that an item of prior art need not identify an allegedly anticipating circuit as

---

[1] The parties are very familiar with the prior art references, so I need not use full citations.

a multiplexer if the circuit's structure is identical to claims 16 or 17. I agree with defendants that the label attached to an item of prior art is not relevant to the anticipation analysis. Further, a reference may be anticipatory even "if, after disclosing the invention, the reference then disparages it. Thus, the question whether a reference 'teaches away' from the invention is inapplicable to an anticipation analysis." Celeritas Technologies, Ltd. v. Rockwell Int'l Corp., 150 F.3d 1354, 1361 (Fed. Cir. 1998) (citation omitted). Although plaintiff presented substantial evidence that circuit designers believed that parallel multiplexer circuits were faster than serial multiplexer circuits, that evidence is relevant to obviousness but not anticipation.

An item of prior art also may inherently anticipate the claimed invention even if it does not expressly include all the limitations of the disputed claim. "Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates." Atlas Powder Co. v. IRECO Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999). "A claim limitation is inherent in the prior art if it is necessarily present in the prior art, not merely probably or possibly present." Akamai Technologies, v. Cable & Wireless Internet Services, Inc., 344 F.3d 1186, 1192 (Fed. Cir. 2003) (citing Rosco v. Mirror Lite, 304 F.3d 1373, 1380 (Fed. Cir. 2002))

Anticipation analysis starts with claim construction. Toro Co. v. Deere & Co., 03-1160, 1161, 2004 WL 78020, at *5 (Fed. Cir. Jan. 20, 2004). Here, the jury was instructed that a "multiplexer" was a "circuit that accepts a plural number (N) of

input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals." The jury was instructed that the phrase "one of the second stage input terminals coupled to the first stage output terminal" "means that the first stage output terminal cannot also be coupled to other circuitry such that the overall result is not a N:1 multiplexer circuit." The jury received analogous instructions that the second and third stage output terminals cannot also be coupled to other circuitry if the result would not be a N:1 multiplexer circuit. The jury heard conflicting expert testimony on whether the prior art circuits cited by defendants as anticipatory were N:1 multiplexer circuits.

The prior art includes 3:1 multiplexers that use serial transmission gate multiplexers (TGMs) in an arrangement similar to claim 15 of the '666 Patent. In a 3:1 multiplexer, however, a serial arrangement of TGMs is necessarily identical to the conventional parallel arrangement. Items of prior art disclosing 3:1 multiplexers that use serial TGMs therefore do not anticipate claims 16 and 17 of the '666 Patent.

Defendants presented evidence that circuits described in the prior art are similar to the circuits described by claims 16 and 17. However, plaintiff presented substantial evidence that the prior art circuits cited by defendants, although similar in structure to plaintiff's serial multiplexer circuits, did not and could not function as N:1 multiplexer circuits.

For example, defendants contended that the 4:1 multiplexer circuit described in the Oklobdzija prior art reference was structural identical to the 4:1 multiplexer circuit disclosed in claim 16 of the '666 Patent. However, plaintiff presented substantial evidence, mainly through expert testimony, that the 4:1 multiplexer described in the Oklobdzija reference lacked essential features of the 4:1 multiplexer described by claim 16. The Oklobdzija reference does not disclose the use of TGMs; has three, not four, different input signals; and uses only two control lines.

Similarly, plaintiff presented substantial evidence that the prior art adder circuits cited by defendants used "live" intermediate outputs that were necessary to their function as adder circuits. The jury could reasonably find that because of the live intermediate outputs, the adder circuits cited by defendants operated effectively as 4:3 or 5:4 circuits, rather than 4:1 or 5:1 multiplexer circuits. There also was substantial evidence that the logic circuits described in the JP '219 and Gorai references used constant signals as input and control signals, rather than the variable signals used in claims 16 and 17 of the '666 Patent.

Defendants disputed plaintiff's expert testimony, and attempted to demonstrate graphically that prior art circuits were structurally identical to claims 16 and 17. I conclude, however, that defendants failed to carry their burden on this motion because the jury's verdict on anticipation was supported by substantial evidence.

III. Motion for Judgment as a Matter of Law on Obviousness

A. Standards for Obviousness

A patent is invalid for obviousness if "differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a) (1994). "Throughout the obviousness determination, a patent retains its statutory presumption of validity, see 35 U.S.C. § 282, and the movant retains the burden to show the invalidity of the claims by clear and convincing evidence as to underlying facts." Rockwell Int'l. Corp. v. United States, 147 F.3d 1358, 1364, 47 USPQ2d 1027, 1031-32 (Fed. Cir. 1998).

Although it is well settled that the ultimate determination of obviousness is a question of law, it is also well understood that there are factual issues underlying the ultimate obviousness decision. Richardson-Vicks Inc. v. Upjohn Co., 122 F.3d 1476, 1479, 44 USPQ2d 1181, 1183 (Fed. Cir. 1997). Specifically, the obviousness analysis is based on four underlying factual inquiries, the well-known Graham factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations, if any, of

nonobviousness. Graham v. John Deere Co., 383 U.S. 1, 7-18, 86 S. Ct. 684, 15 L. Ed.2d 545 (1966); Kegel Co., Inc. v. AMF Bowling, Inc., 127 F.3d 1420, 1430, 44 USPQ2d 1123, 1130 (Fed. Cir. 1997).

McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1349 (Fed. Cir. 2001). When a court submits obviousness to the jury, the court should presume that "that the jury resolved the underlying factual disputes in favor of the verdict winner and leave those presumed findings undisturbed if they are supported by substantial evidence." Jurgens v. McKasy, 927 F.2d 1552, 1557 (Fed. Cir. 1991) (citation omitted).

B. Discussion

Defendants argue that it would have been obvious to one skilled in the art that omitting intermediate outputs from adder circuits would create 4:1 and 5:1 serial multiplexer circuits. Plaintiff, however, presented substantial evidence that before the '666 Patent was issued, conventional wisdom counseled against multiplexer circuits using serial TGMs. Persons skilled in the art believed that for optimum speed, which is always a priority in circuit design, multiplexer circuits should use a parallel or "tree" structure that minimized the number of stages in the circuit. There was an assumption that the additional stages required for a 4:1 or 5:1 serial multiplexer circuit would make it slower than a 4:1 or 5:1 parallel multiplexer. Contrary to that wisdom, plaintiff's design maximized the number of stages, yet allegedly tested

faster in some applications than conventional parallel multiplexer circuits.

Plaintiff also presented secondary evidence of nonobviousness. Even putting that evidence aside, however, evidence that conventional wisdom "taught against" plaintiff's' proposed serial design was sufficient to defeat defendants' claim of obviousness.

DEFENDANTS' MOTION FOR NEW TRIAL

Defendants move for a new trial, arguing that this court improperly excluded evidence of the reexamination proceedings; that the jury instructions and the verdict form were fatally flawed; and that this court abused its discretion on evidentiary issues.

I. Standards for Motion for a New Trial

The court may grant a motion for new trial if the jury's verdict is contrary to the clear weight of the evidence, if the verdict is based on false evidence, or if there would otherwise be a miscarriage of justice. See Roy v. Volkswagen of America, Inc., 896 F.2d 1174, 1176 (9th Cir.), as amended by 920 F.2d 618 (9th Cir. 1990). "While the trial court may weigh the evidence and credibility of the witnesses, the court is not justified in granting a new trial 'merely because it might have come to a different result from that reached by the jury.'" Id. (quoting Wilhelm v. Associated Container Transp. (Australia) Ltd., 648 F.2d, 1197, 1198 (9th Cir. 1981)). The district court has discretion in deciding whether to grant a new trial. Unocal Corp. v. United States, 222 F.3d 528, 534, (9th Cir. 2000).

II. Discussion

A. Exclusion of Evidence on Reexamination Proceedings

Defendants contend that I should not have excluded evidence of the extended reexamination proceedings on the '666 Patent. In the fifth and final reexamination proceeding, the Patent and Trademark Office (PTO) concluded that as amended, claims of the '666 Patent was invalid. Plaintiff is appealing the PTO's ruling to the Board of Patent Appeals and Interferences. If the Board affirms the PTO's ruling, plaintiff could appeal to the Federal Circuit.

Defendants contend that they were prejudiced by exclusion of the reexamination history because at the trial on validity here plaintiff could evade admissions made during the reexamination proceedings. Defendants argue that the reexamination history was probative of issues in dispute at trial, including suggestions in the prior art to combine references, and the motivation of persons skilled in the art to extend 3:1 serial TGMs to create 4:1 or 5:1 serial TGMs.

I agree, however, with plaintiff that admitting the reexamination history into evidence would have confused rather than assisted the jury. The reexamination history was complex, including five separate proceedings. Plaintiff submitted amended claims that differed from the original claims at issue here. The volume of paper alone, several thousand pages, was massive.

Had the reexamination record been admitted, the jury would have needed instructions on the PTO's role in reexamination proceedings, including legal presumptions and standards that would not apply to court challenges. There was also a danger that the jury would improperly defer to the PTO's conclusion on validity. I conclude that excluding evidence of the reexamination proceedings was not an abuse of discretion. Even if exclusion was error, defendants were not prejudiced because they did not need evidence from the reexamination proceedings to make their arguments based on prior art.

B. Jury Instructions

Defendants contend that several jury instructions were incorrect. Defendants also contend that the instructions as a whole were fatally flawed.

1. Standards

"A court must formulate jury instructions so that they fairly and sufficiently address the issues a case presents, accurately state the law, and are not misleading." Mena v. City of Simi Valley, 332 F.3d 1255, 1267 (9th Cir. 2003) (citing Duran v. City of Maywood, 221 F.3d 1127, 1130 (9th Cir. 2000)). In evaluating jury instructions, the court should consider the instructions as a whole. Guebara v. Allstate Ins. Co., 237 F.3d 987, 992 (9th Cir. 2001).

2. Claim Construction Issues

Defendants contend that the jury instructions construing the claim terms "control signal" and "output terminal coupling" were incorrect. I based

jury instructions regarding claim construction on the special master's reports and recommendations.

I adhere to my conclusion that the special master's claim construction is correct.

3. Presumption of Validity

Defendants object to the failure to give their proposed instruction on the presumption of validity. The jury received a standard instruction on the presumption.

Defendants' proposed instruction included a description of the patent examiner's role and stated that no deference was due the examiner if the examiner failed to consider material prior art before issuing the patent. Defendants' proposed instruction also stated that prior art which was not considered by the examiner does not change defendants' burden of proof but may so clearly invalidate a patent that defendants satisfy their burden "merely by proving the existence of that prior art."

As plaintiff notes, the jury was not instructed that the patent examiner was entitled to deference. Defendants' proposed instruction could have confused the jury on the applicable standards and burden of proof.

4. Intermediate Outputs

Defendants object to the jury instruction giving the claim construction for the term "intermediate outputs." The jury was given the special master's original claim construction, which defendants contend was sufficient for lawyers but too

difficult for jurors to comprehend. I adhere to the special master's well-reasoned claim construction.

5. Inherency and Anticipation

Defendants contend that the jury instruction on inherent anticipation erroneously required that a person of ordinary skill in the art understand at the time of the invention that a feature was inherently present in the item of prior art. The instruction given, which was from the Federal Circuit Bar Association model instruction no. 10.8, stated, "Something is inherent in an item of prior art if it is always present in the prior art or always results from the practice of the prior art, and if a skilled person would understand that to be the case."

I agree with defendants that anticipation by inherency does not require that a person of ordinary skill would have recognized the inherent element at the time of the invention. "[T]he fact that a characteristic is a necessary feature or result of a prior-art embodiment (that is itself sufficiently described and enabled) is enough for inherent anticipation, even if that fact was unknown at the time of the prior invention." Toro Co., 2004 WL 78020, at *6 (citations omitted); Schering Corp. v. Geneva Pharmaceuticals, Inc., 339 F.3d 1373, 1377 (Fed. Cir. 2003) ("recognition by a person of ordinary skill in the art before the critical date . . . is not required to show anticipation by inherency.").

The instruction given here correctly required, that inherent anticipation be clear to a person of ordinary skill in the art. The instruction did not, however, expressly state that a person of ordinary

skill in the art need not have understood that the element was inherent in the prior art when the patented invention was filed. This omission, even assuming it as abuse of discretion, did not prejudice defendants under the facts here.

6. Commercial Success and Copying

Defendants object to the jury instructions on commercial success and copying, which are among the objective indications of nonobviousness. The jury instructions stated that commercial success must be "caused by the merits of the claimed invention" and that "commercial success is relevant to obviousness only if the success of the product is related to a feature of the patent claims at issue here." Defendants contend that the instructions should have stated that commercial success was "due to" the patented feature. The instructions given, however, also stated that the jury should not consider commercial success if the success was caused by something other than the patented feature, such as innovative marketing. I conclude that the jury instructions on commercial success were adequate.

Defendants object to the instruction on copying, arguing that the instruction should have required that defendants intended to copy the patented invention. I conclude that the instruction given was not so prejudicial as to require a new trial.

7. Instructions As a Whole

Defendants argue that the instructions as a whole were so flawed as to require a new trial. The law does not require perfect jury instructions. I

conclude that the jury instructions given here were at least adequate.

C. Verdict Form

The jury received a verdict form similar to the one submitted by plaintiff, which asked simply whether claims 16 or 17 were obvious in light of the specified items of prior art. Defendants submitted a complex verdict form that identified each possible combination of prior art that could have rendered claims 16 or 17 obvious.

The verdict form given the jury was clear, concise, and avoided the danger of inconsistent verdicts. The detailed verdict form that defendants proposed was not necessary.

D. Evidentiary Rulings

Defendants contend that this court made erroneous evidentiary rulings. The trial court has discretion in making evidentiary rulings. Defenders of Wildlife v. Bernal, 204 F.3d 920, 927 (9th Cir. 2000). An evidentiary error justifies reversal if it is not only an abuse of discretion but also prejudicial. Id. at 927-28.

1. Meeting Between Inventor and Defendants

Defendants object to admission of the inventor's notes on a 1997 meeting with defendants' representatives, contending that these notes are inadmissible under Federal Rule of Evidence 408. Rule 408 generally excludes "[e]vidence of conduct or statements made in compromise negotiations."

Defendants cite an August 1997 letter to defendants from Marvin Bush, who was then plaintiff's president, stating that one purpose of the February 1997 meeting was to "inform Hitachi" of alleged infringement of plaintiff's '666 Patent.

I agree with plaintiff that the inventor's notes of the meeting with defendants were admissible because plaintiff had not yet made a claim of infringement at that time. See Deere & Co. v. International Harvester Co., 710 F.2d 1551, 1557 (Fed. Cir. 1983) (exclusion of evidence under Rule 408 limited to "actual disputes over existing claims"; party's offer to license patent admissible because no accompanying charge of infringement). Cf. Red Wing Shoe Co. v. Hockerson-Halberstadt, Inc., 148 F.3d 1355, 1361 (Fed. Cir. 1998).

Defendants also argue that the inventor's notes were inadmissible hearsay. However, the inventor took the notes in the regular course of business, and statements by defendants' representatives are admissible as the admissions by a party opponent. Even if the notes themselves were not admissible, admission of the notes was harmless because the inventor was entitled to testify about statements he had heard.

2. Testing Documents on Claimed Invention

Defendants contend that it was error to admit documents showing testing of plaintiff's claimed invention by third parties before plaintiff filed the patent application. Defendants cite the rule of corroboration, which prohibits a party from proving

the conception of an invention solely through the inventor's testimony. See Shu-Hui Chen v. Bouchard, 347 F.3d 1299, 1309-10 (Fed. Cir. 2003). Plaintiff responds that the testing documents were admissible because the rule excludes only the oral testimony of the putative inventor. I agree with plaintiff that the rule does not bar these documents because plaintiff submitted them to show secondary considerations relevant to obviousness, not to establish priority.

Defendants also contend that exhibits concerning test results were inadmissible hearsay. Plaintiff responds that these documents were not offered to show that the statements were true, but rather to show that the third parties who performed the tests considered plaintiff' proposed invention to be potentially valuable. I conclude that the testing documents were admissible. Even if the admission was erroneous, it did not seriously prejudice defendants.

3. Evidence of Copying

Defendants contend it was error to admit evidence that defendants manufactured microprocessors incorporating 4:1 and 5:1 serial multiplexers that were allegedly identical to plaintiff's invention. I ruled that such evidence was relevant to obviousness.

Although such evidence might appear to bear on infringement, which was not at issue in this phase of the litigation, infringement is not the same as merely copying a patented device. "While copying may be relevant to obviousness, it is of no import on

the question of whether the claims of an issued patent are infringed." Allen Eng'g Corp. v. Bartell Indus., Inc., 299 F.3d 1336, 1351 (Fed. Cir. 2002). Evidence that defendants copied plaintiff's invention was relevant and admissible on obviousness. The jury was instructed during the trial that infringement was not at issue.

CONCLUSION

Defendants' motions for a new trial (#383) and for judgment as a matter of law (##377, 379) are denied. Claims 16 and 17 of plaintiff's '666 Patent are not invalid for obviousness.

DATED this 9 day of February, 2004.

/s/ Owen M. Panner

OWEN M. PANNER
U.S. DISTRICT JUDGE

APPENDIX I

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF OREGON

[Filed OCT. 28, 2003]

TRANSLOGIC TECHNOLOGY, INC.,	)	
Plaintiff,	)	Civil Action No. 99-407-PA
v.	)	
HITACHI, LTD., HITACHI AMERICA, LTD., RENESAS TECHNOLOGY AMERICA, INC.,	)	VERDICT FORM
Defendants.	)	

We, the duly-impaneled jury in the above-entitled case, find as follows:

1. Has Hitachi proved by clear and convincing evidence that claim 16 of the '666 Patent is invalid because it was anticipated by one or more prior art references?

Yes___ No_X_

If your answer to question #1 is "No," then skip to question #3.

2. If your answer to question #1 is "Yes," check the appropriate box next to each of the following references that you find anticipates claim 16 of the '666 Patent.

Gorai et al., "Automated Synthesis of Combination Circuits by Cascade Networks of Multiplexers"	Yes___	No___
Japanese Patent Appln. No. H1244,531 ("Goto '531")	Yes___	No___
Japanese Patent Appln. No. H1256,219 ("Goto '219")	Yes___	No___
Japanese Patent Appln. No. H1281,529 ("Goto '529")	Yes___	No___
"Oklobdzija"	Yes___	No___

3. Has Hitachi proved by clear and convincing evidence that claim 17 of the '666 Patent is invalid because it is anticipated by one or more prior art references?

Yes___ No_X_

If your answer to question #3 is "No," then skip to question #5.

4. If your answer to the previous question is "Yes," check the appropriate box next to each of the following references that you find anticipates claim 17 of the '666 Patent.

Gorai et al., "Automated Synthesis of Combination Circuits by Cascade Networks of Multiplexers"	Yes___	No___
Japanese Patent Appln. No. H1244,531 ("Goto '531")	Yes___	No___
Japanese Patent Appln. No. H1256,219 ("Goto '219")	Yes___	No___
Japanese Patent Appln. No. H1281,529 ("Goto '529")	Yes___	No___
"Oklobdzija"	Yes___	No___

5. Has Hitachi proved by clear and convincing evidence that claim 16 of the '666 Patent is invalid because it was obvious in light of one or more prior art references?

Yes___ No _X_

6. Has Hitachi proved by clear and convincing evidence that claim 17 of the '66 Patent is invalid because it was obvious in light of one or more prior art references?

Yes___ No _X_

Dated this _27_ day of October, 2003.

Signed: /s/ Marion J. Anderson

Presiding Juror

Printed Name: Marion J. Anderson

APPENDIX J

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

06-1192
(Re-examination Nos. 90/005,384; 90/005,823; 90/005,881; 90/006,051 and 90/006,392)

IN RE TRANSLOGIC TECHNOLOGY, INC.

ORDER

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

ORDER

A combined petition for panel rehearing and for rehearing en banc having been filed by the Appellant, and a response thereto having been invited by the court and filed by the Appellee,* and the petition for rehearing and response, having been referred to the panel that heard the appeal, and thereafter the petition for rehearing en banc and response having been referred to the circuit judges who are in regular active service,

UPON CONSIDERATION THEREOF, it is

ORDERED that the petition for panel rehearing be, and the same hereby is, DENIED and it is further

ORDERED that the petition for rehearing en banc be, and the same hereby is, DENIED.

The mandate of the court will issue on January 31, 2008.

Chief Judge Michel did not participate in the vote.

FOR THE COURT,

s/Jan Horbaly/JB

Jan Horbaly

Clerk

Dated: 01/24/2008

cc: Richard L. Rainey
Stephen Walsh, James G. Gilliland, Jr.

IN RE TRANSLOGIC TECHNOLOGY, 2006-1192 (PTO - 90/005,384)

FILED

U.S. COURT OF APPEALS FOR THE FEDERAL CIRCUIT

JAN 24 2008

JAN HORBALY

CLERK

*Response also filed on behalf of the Intervenor, Hitachi, Ltd., et al.

APPENDIX K

United States Court of Appeals

for the Federal Circuit

2006-1192

(Re-examination Nos. 90/005,384;
90/005,823; 90/005,881;
90/006,051 and 90/006,392)

IN RE TRANSLOGIC TECHNOLOGY, INC.

Jeffrey S. Love, Klarquist Sparkman, LLP, of Portland, Oregon, argued for appellant. With him on the brief were Jared S. Goff and John D. Vandenberg.

William LaMarca, Associate Solicitor, Office of the Solicitor, United States Patent and Trademark Office, of Arlington, Virginia, argued for the Director of the United States Patent and Trademark Office. With him on the brief was Thomas W. Krause, Associate Solicitor.

James G. Gilliland, Jr., Townsend and Townsend and Crew LLP, of Palo Alto, California, argued for intervenors Hitachi Ltd., et al. With him on the brief were Madison C. Jellins and D. Stuart Bartow. Of counsel on the brief were Nathan Lane

III and David S. Elkins, Squire, Sanders & Dempsey L.L.P., of Palo Alto, California; David Axelrod, Schwabe, Williamson & Wyatt, P.C., of Portland, Oregon; and Alan R. Loudermilk, Loudermilk & Associates, of Cupertino, California.

Appealed from: United States Patent and Trademark Office

Board of Patent Appeals and Interferences

United States Court of Appeals

for the Federal Circuit

2006-1192

(Re-examination Nos. 90/005,384; 90/005,823; 90/005,881; 90/006,051 and 90/006,392)

IN RE TRANSLOGIC TECHNOLOGY, INC.

DECIDED: October 12, 2007

Before MAYER, RADER, and PROST, Circuit Judges.

RADER, Circuit Judge.

The United States Patent and Trademark Office's Board of Patent Appeals and Interferences ("Board") upheld the examiner's rejection of U.S. Patent No. 5,162,666 ("the '666 patent") in a reexamination proceeding, Appeal No. 2005-1050. Because the '666 patent would have been obvious at the time of invention, this court affirms.

I

The United States Patent and Trademark Office issued the '666 patent, entitled "Transmission Gate Series Multiplexer", on November 10, 1992 from an application filed on March 15, 1991. In addition to this appeal from the Board's decision, the '666 patent is the subject of a patent infringement litigation between Translogic Technology, Inc. ("Translogic") and Hitachi, Ltd. et al. ("Hitachi") in the United States District Court for the District of Oregon. The district court case began on March 24, 1999. Thereafter, on June 4, 1999 and ending on September 27, 2002, Hitachi filed five third-party requests for reexamination of the *'666* patent. The Patent Office merged the various requests into a single proceeding. On March 8, 2004, the merged reexamination resulted in the rejection of claims 16, 17, 39-45, 47 and 48 under 35 U.S.C. § 103(a) because they would have been obvious at the time of invention. The Patent Office found the claims obvious in light of the references Gorai or Tosser in view of Weste. During the reexamination proceedings, Translogic cancelled original claims 1-15 and 18-27, and newly added claims 28-38 and 46. Translogic then appealed to the Board. On July 14, 2005, the Board affirmed the rejection. The Board denied Translogic's request for reconsideration. Translogic then appealed the Board's decision to this court.

During this entire reexamination process, the district court infringement case proceeded in parallel. In October 2003, a jury upheld the patent as valid. In February 2005, the district court granted

summary judgment of infringement with respect to some, but not all, of Hitachi's accused products. In May 2005, a jury found Hitachi had induced infringement and held Hitachi liable for $86.5 million in damages. The district court entered a permanent injunction, which, after Hitachi's interlocutory appeal, this court stayed.

After post-trial briefing, the district court entered final judgment against Hitachi in December 2005. Hitachi appealed to this court. This court consolidated the interlocutory appeal with the appeal from the final judgment and added Translogic's reexamination appeal from the Board to the same panel. This opinion only addresses Translogic's reexamination appeal from the Board.

The '666 patent deals with multiplexers. A multiplexer is a type of electrical circuit. A multiplexer has multiple inputs, one or more control lines, and one output. The signals on the control lines select one of the various inputs to be passed to the output. In a 2:1 multiplexer, a single output value is selected from two inputs. Similarly, in 4:1 and 8:1 multiplexers, a single output is selected from among four or eight inputs, respectively. Thus, the invention selects one of the multiple inputs to pass to the output.

The number of control lines (x) for a conventional multiplexer depends on the number of inputs to the multiplexer. Generally, a given number of control lines (x) can select one output from among maximum of 2^x inputs. In a 2:1 multiplexer, a single control line (x = 1) can select between 2^1 or 2 inputs,

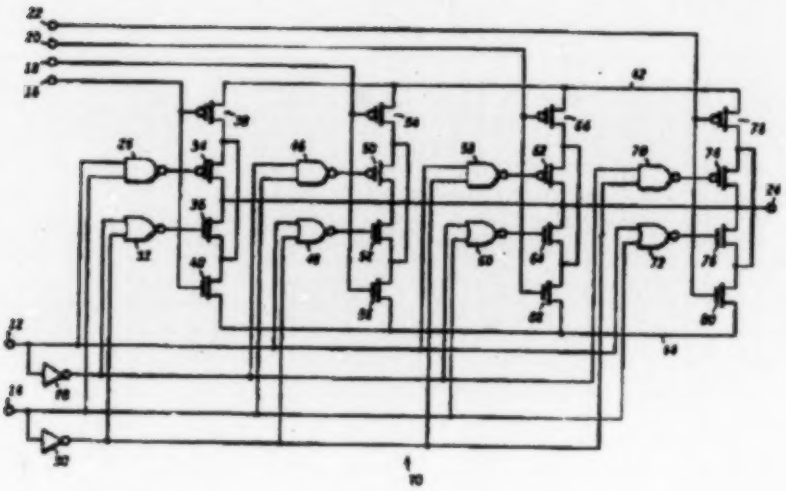
therefore x = 1. In a 4:1 multiplexer, two control lines (x = 2) are used to select among 2^2 or 4 inputs, and in an 8:1 multiplexer, three control lines (x = 3) can select between 2^3 or 8 inputs.

Figure 1 of U.S. Patent No. 5,012,126 (referenced by the '666 patent) shows a 4:1 conventional multiplexer. Lines 16, 18, 20 and 22 are inputs, lines 12 and 14 are control lines and line 24 is the output. The control lines will select which input (i.e., 16, 18, 20 or 22) to pass to the output. This particular circuit passes the inverse of the selected input to the output.[1] For example, if line 12 is a logic 0 and line 14 is a logic 1, then the circuit passes the inverse of the signal on line 18 to output line 24. As another example, if line 12 is a logic 1 and line 14 is a logic 1, then the circuit passes the inverse of the signal on line 16 to output line 24.

---

[1] The inverse of a signal is often used in circuits and does not change the multiplexer function.

BEST AVAILABLE COPY



Control Line 12	Control Line 14	Output 24
0	0	Inverse of Line 22
1	0	Inverse of Line 20
0	1	Inverse of Line 18
1	1	Inverse of Line 16

The '666 patent describes a multiplexer that couples together multiple stages of 2:1 multiplexers in series. The '666 patent specifically uses a transmission gate multiplexer ("TGM") as each 2:1 multiplexer. Figure 3 of the '666 patent (see below) illustrates a 4:1 series multiplexer that connects three TGMs (i.e., A, B and C) in series. The inputs are 10, 11, 12 and 13, the output is Z and the control lines are S1, S2 and S3. While a conventional 4:1

multiplexer would have two control lines, the 4:1 series multiplexer, according to the '666 patent configuration, has three control lines.

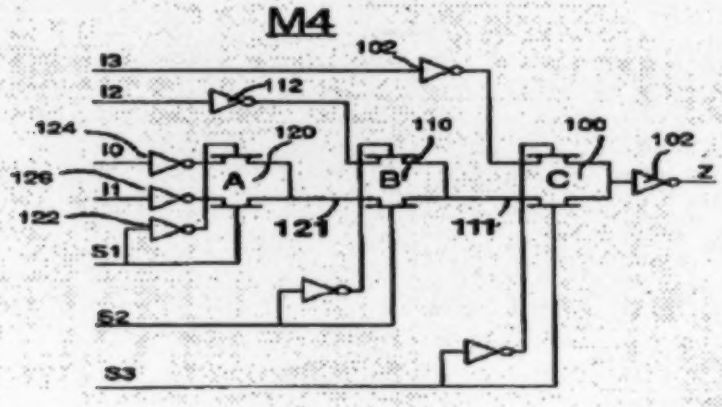


FIG 3

In the figure above, lines S1, S2, and S3 are control lines and lines 10, 11, 12, and 13 are input lines. The series multiplexer operates in cascade by passing the selected input to the output in a series of selections. For example, for the input on 11 to be passed to output Z, S1 must be a logic 1 to pass 11 to the input of TGM B on line 121, S2 must also be a logic 1 to pass 11 to the input of TGM C via line 111, and finally S3 must be a logic 1 to pass the output of TGM B to the output of TGM C. In other words, the line 1 input must prevail in each selection phase. In another example, 13 would be passed to the output Z by setting S3 to logic 0. When the signal on S3 is a logic 0, control lines S1 and S2 do not influence the output because TGM C will pass the value on 13 directly from the input line 13 to the output Z.

The claims on appeal specify multiplexers with multiple 2:1 TGMs connected in series. In the series configuration, the output of one TGM connects

to one input of the next TGM. Each TGM is known as a stage. A multiplexer built from a series of TGMs has p control inputs and (p+1) data inputs for a total of (2p+1) overall inputs. For example, a 4:1 series multiplexer has p=3 control inputs and 4 data inputs thereby resulting in 7 ((2*3) + 1 = 7) overall inputs whereas a conventional 4:1 multiplexer has 4 inputs and 2 control inputs, resulting in 6 overall inputs. During the reexamination, Translogic agreed that all of the claims on appeal stood or fell with claims 47 and 48:

47. A multiplexer circuit comprising:

a first stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

the first and second signal input terminals coupled to receive first and second input variables, respectively;

the control input coupled to receive a first control signal;

a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the second stage input terminals coupled to the first stage output terminal; the other one of the second stage signal input terminals coupled to receive a third input variable;

the second stage control input terminal

coupled to receive a second control signal;

a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the third stage input terminals coupled to the second stage output terminal;

the other one of the third stage input terminals coupled to receive a fourth input variable;

and the third stage control input variable coupled to receive a third control signal whereby the circuit forms a 4:1 multiplexer.

48. A multiplexer circuit comprising:

a first stage TGM circuit having first and second signal input terminals, a control input terminal, and an output terminal;

the first and second signal input terminals coupled to receive first and second input variables, respectively;

the control input terminal coupled to receive a first control signal;

a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the second stage signal input terminals coupled to the first stage output terminal;

the other one of the second stage signal input terminals coupled to receive a third input variable;

the second stage control input terminal coupled to receive a second control signal;

a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the third stage signal input terminals coupled to the second stage output terminal;

the other one of the third stage signal input terminals coupled to receive a fourth input variable;

the third stage control input terminal coupled to receive a third control signal;

a fourth stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the fourth stage signal input terminals coupled to the third stage output terminal;

the other one of the fourth stage signal input terminals coupled to receive a fifth input variable; and

the fourth stage control input terminals coupled to receive a fourth control signal; whereby the circuit forms a 5:1

multiplexer.

The Board affirmed the rejection of claims 47 and 48 as obvious under § 103(a). In applying the obviousness test, the Board relied on Gorai combined with Weste, as well as Tosser combined with Weste. The Gorai and Tosser references are technical articles; the Weste reference is a textbook:

Gorai, R.K., and Pal, A., Automated synthesis of combinational circuits by cascade networks of multiplexers, IEE Proc., Vol. 137, Pt. E, No. 2, March 1990, pages 164-170.

Weste, Neil H.E., and Eshraghian, Kamran, Principles of CMOS VLSI Design: A Systems Perspective (Addison-Wesley Publ. Co. 1985), pages 14-17 and 172-175.

Tosser, A.J., and Aoulad-Syad, D., Cascade networks of logic functions built in multiplexer units, IEE Proc., Vol. 127, Pt. E, No. 2, March 1980, pages 64-68.

The Board found that Fig. 3 of Gorai (see below) discloses a three-stage multiplexer circuit with four inputs (h_p, g_p, h_{p-1}, h_i) and three control inputs. (x_p, x_{p-1} and x_i).

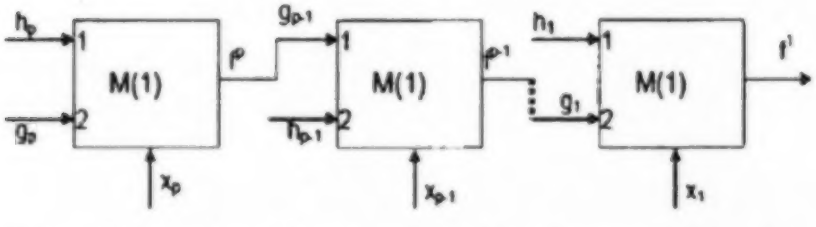


Fig. 3 A cascade network of p-stages of M(1)s

The Board found that Gorai does not disclose use of TGMs for each multiplexer stage (i.e., M(1)) in Fig. 3. The Board, however, found that Weste taught a 2:1 TGM circuit to transfer a logic 0 or a logic 1 between the input and output. The Weste reference discloses and teaches a TGM in its Figs. 1.10 (a) and (b). The figures show the use of complementary switches to pass logic Os and logic 1s.

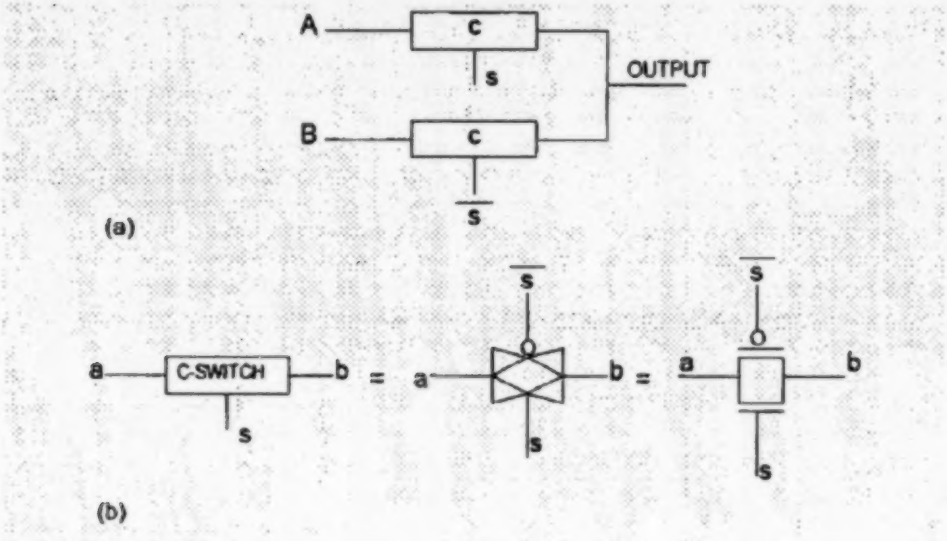


Fig. 1.10. A CMOS 2-input multiplexer

The Board thus found that a person of ordinary skill in the art would have been motivated to use a TGM circuit as taught in Weste for the multiplexer stages in Gorai.

The Board also found that Fig. 9 of Tosser (see below) teaches a 4:1 multiplexer built from three 2:1 multiplexer stages connected in series.

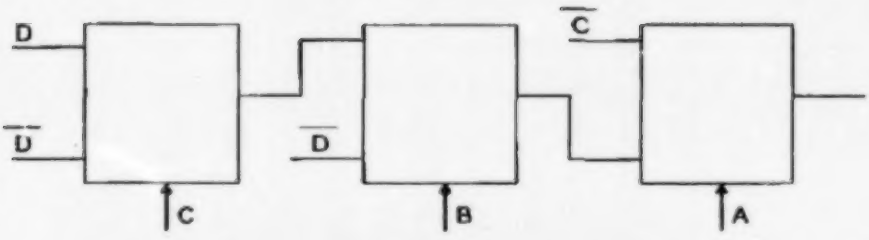


Fig. 9 Cascade 2-input MUX network derived from Fig.

Like the Gorai reference, Tosser does not disclose the use of TGMs for the multiplexer stages. Once again, the Board found that a person of ordinary skill in the art would have been motivated to use a TGM circuit as taught in Weste for the multiplexer stages in Tosser.

While the Board interpreted a number of claim terms during its proceedings, one claim term is important for this appeal. The Board interpreted the term "coupled to receive" in the claim phrase "control input terminal 'coupled to receive' a control signal" as a "[t]erminal capable of receiving a control signal. The control signal itself is not part of the claimed structure." Ex parte Transloqic Tech., Inc., Appeal No. 2005-1050, Board of Patent Appeals and Interferences (May 31, 2005).

II

This court reviews claim construction without deference. Cybor Corp. v. FAS Techs. Inc., 138 F.3d 1448, 1456, 46 USPQ2d 1169, 1174 (Fed. Cir. 1998) (en banc); Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995), aff'd, 517 U.S. 370 (1996). "[D]uring examination proceedings, claims

are given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372 (Fed. Cir. 2000).

Section 103 within title 35 of the U.S. Code "forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" KSR Int'l Co. v. Teleflex Inc., 550 U.S. ----; 127 S.Ct. 1727, 1734 (2007); (quoting 35 U.S.C. § 103). "Determination of obviousness under 35 U.S.C. § 103 is a legal conclusion based on underlying facts." In re Kumar, 418 F.3d 1361, 1365 (Fed. Cir. 2005). This court reviews "the Board's ultimate determination of obviousness de novo." In re Kotzab, 217 F.3d 1365, 1369 (Fed. Cir. 2000). However, the Board's underlying findings of fact receive review for substantial evidence. Id. "If the evidence in [the] record will support several reasonable but contradictory conclusions, we will not find the Board's decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative." In re Jolley, 308 F.3d 1317, 1320 (Fed. Cir. 2002).

III

Translogic puts forth three major arguments that the Board erred in holding the claims of the '666 patent obvious over Gorai in view of Weste. First, Translogic contends that the Board incorrectly construed the claim term "coupled to receive."

Second, Translogic contends that the Gorai reference is not relevant prior art with respect to the '666 patent. Third, Translogic contends that the Gorai reference does not disclose the use of TGMs, or in other words, that the record shows no motivation, in Weste or otherwise before the time of invention, to use TGMs for circuits in series. In effect, the Weste reference merely describes TGMs but does not suggest their use in this purported inventive combination.

The Board construed the term "coupled to receive" signals to mean terminals merely "capable of receiving" signals. Translogic argues that the Board should follow the claim construction in the companion infringement case from the United States District Court for the District of Oregon. The Oregon District Court determined that "signal input terminal 'coupled to receive' an input variable" would mean "connected to receive an input variable, directly or through one or more intervening inverters or buffers." Translogic Tech., Inc. v. Hitachi, Ltd., Hitachi America, Ltd., and Renesas Tech. America, Inc., Civ. No. 99-407-PA (D. Or. May 12, 2005) (Claim Construction Chart). Under this construction, representative claims 47 and 48 require each input and control input terminal to be connected to receive a variable signal from a different source. Thus, according to Translogic, the Gorai reference does not disclose that each input and control input terminal must receive a variable signal from a different source. Instead, according to Translogic, Gorai teaches logic circuits with input terminals coupled to share signals and receive constants.

In Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc), this court set forth the best practices for claim construction. According to that decision, the words of a claim "are generally given their ordinary and customary meaning." Id. at 1312. The ordinary and customary meaning "is the meaning that the term would have to a person of ordinary skill in the art in question." Id. at 1313. For this reason, "claims must be read in view of the specification, of which they are a part." Id. at 1315. (internal quotations omitted). The specification "is the single best guide to the meaning of a disputed term." Id.

Representative claim 47, like representative claim 48, clearly claims a multiplexer circuit with a number of 2:1 TGMs connected in series. While claim 47 specifies a 4:1 multiplexer, claim 48 specifies a 5:1 multiplexer. Both claims specify that the multiplexer circuit connects 2:1 TGMs in series. Thus, under the terms of the patent, an N:1 multiplexer connects (N-1) TGMs in series with each TGM controlled by a corresponding (N-1) control input signal. '666 Patent col.3 11.63-66. Fig. 3 from the '666 patent shows the claimed circuit for the 4:1 multiplexer.

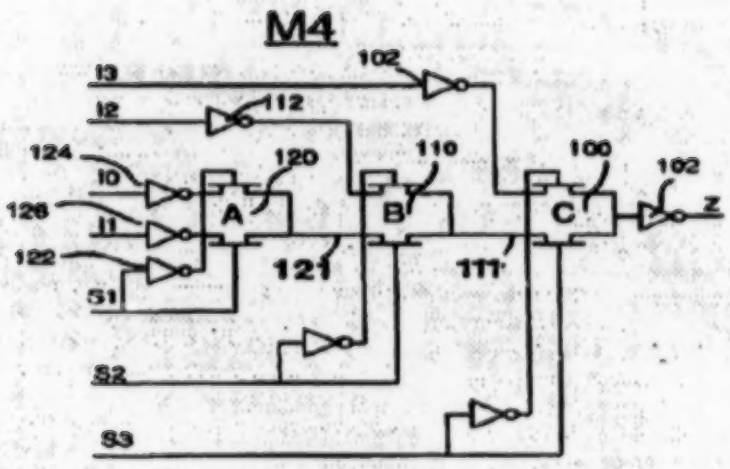


FIG 3

The words of the claim coupled with the specification define the term "input terminals 'coupled to receive' first and second input variables." First, the claim terms do not specify any structural connection for the input terminals. Furthermore, Fig. 3 of the '666 patent and the other figures show no structural connection for the input terminals (i.e., I0, I1, ... I(N-1)) or the control input terminals (i.e., S1, S2, S3). In fact, Translogic admits, as is proper for a structural circuit, that the input variables (i.e., signals) are not part of the claimed invention.

A claim language comparison also shows the proper construction for the term at issue for the '666 patent. Claim 47 has two similar, but significantly different phrases, "coupled to receive" and "coupled to." The term "coupled to" in the phrase "second stage input terminal 'coupled to' the first stage output terminal" defines a connection between the TGMs. In other words, "coupled to" in the context of this claim phrase defines the connection between two of the TGMs essential for a series multiplexer.

On the other hand, the term "coupled to receive" in the phrase "input terminals 'coupled to receive' first and second input variables" does not specify a particular connection. In other words, the claimed circuit does not require any specific input or connection. Instead, like any logic circuit, this part of the circuit only accepts inputs from an external source. As such, "coupled to" and "coupled to receive" are clearly different in the claimed '666 patent multiplexer circuit. As shown in Fig. 3 of the '666 patent, the input terminals (i.e., I0, I1, ..., I(N-1)) only need to be "capable of receiving" an input variable for the multiplexer circuit as claimed in the '666 patent. Even if the input terminals are not connected, the circuit claimed in the '666 patent defines a series multiplexer. Therefore, this court agrees with the Board's construction that "coupled to receive" means "capable of receiving." With the disputed term limitation decided, this court now turns to obviousness.

An invention is unpatentable as obvious if the differences between the patented subject matter and the prior art would have been obvious at the time of invention to a person of ordinary skill in the art. In re Gartside, 203 F.3d 1305, 1319 (Fed. Cir. 2000). In a recent case, the Supreme Court reiterated the basic principles for an obviousness inquiry. KSR Int'l Co. v. Teleflex Inc., 550 U.S. ----, 127 S.Ct. 1727 (2007). KSR featured rather simple technology - an adjustable throttle pedal for an automobile, the Engelgau patent (U.S. Pat. No. 6,237,565 ("the '565 patent")). Adjustable pedal technology accommodates an automobile throttle to drivers of different heights. This patented technology combined an adjustable

pedal with an electronic sensor to measure the pedal depression. Both of these features were in the prior art. An Asano patent claimed an adjustable pedal like Engelgau; a Rixon patent (as modified by a Smith reference) disclosed electronic calibration features like Engelgau. The PTO had not considered the Asano reference during the prosecution of the Engelgau patent.

When Teleflex sued KSR for infringement, the district court invalidated the '565 patent on summary judgment. This court reversed because the trial court had not made specific findings to show a teaching, suggestion, or motivation to combine ("TSM test"). The Supreme Court, in turn, reversed: "A person having ordinary skill in the art could have combined Asano with a pedal position sensor in a fashion encompassed by claim 4, and would have seen the benefits of doing so." KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1743.

On one level, KSR corrected a rather straightforward error. The error appears right before footnote 3 in this court's opinion:

> In this case, the Asano patent does not address the same problem as the '565 patent. The objective of the '565 patent was to design a smaller, less complex, and less expensive electronic pedal assembly. The Asano patent, on the other hand, was directed at solving the

"constant ratio problem."

Teleflex, Inc. v. KSR Int'l, Co., 119 Fed. App'x. 282, 288 (Fed. Cir. 2005). This passage overlooks the fundamental proposition that obvious variants of prior art references are themselves part of the public domain. See KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1743; Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co., 464 F.3d 1356, 1361 (Fed. Cir. 2006); In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999) ("We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved. . . . "). In the context of KSR, the Asano teachings and its obvious variants were relevant prior art, even if that patent did address a different problem (the constant ratio problem). The Supreme Court highlighted that error in its opinion:

> The primary purpose of Asano was solving the constant ratio problem; so, the court concluded, an inventor considering how to put a sensor on an adjustable pedal would have no reason to consider putting it on the Asano pedal. Common sense teaches, however, that familiar items may have obvious uses beyond their primary purposes, and in

> many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. Regardless of Asano's primary purpose, the design provided an obvious example of an adjustable pedal with a fixed pivot point; and the prior art was replete with patents indicating that a fixed pivot point was an ideal mount for a sensor. The idea that a designer hoping to make an adjustable electronic pedal would ignore Asano because Asano was designed to solve the constant ratio problem makes little sense.

KSR Int'l Co., 550 U.S. at ----, 127 S.Ct. at 1742.

The Supreme Court also criticized this court's "rigid and mandatory" application of the motivation to combine test: "The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents." Id. at 1741. Instead, the Supreme Court advised that "common sense" would extend the use of customary knowledge in the obviousness equation: "A person of

ordinary skill is also a person of ordinary creativity, not an automaton." Id. at 1742. Thus, the Supreme Court set aside any "rigid" application of the TSM test and ensured use of customary knowledge as an ingredient in that equation.

The Supreme Court observed that this court had also "elaborated a broader conception of the TSM test than was applied in [KSR]." Id. at 1743. Specifically the Court referred to Dystar Textilfarben GmbH & Co. v. C.H. Patrick Co., wherein this court noted: "Our suggestion test is in actuality quite flexible and not only permits, but requires, consideration of common knowledge and common sense." 464 F.3d 1356, 1367 (Fed. Cir. 2006) (emphasis original). The Court suggested that this formulation would be more consistent with the Supreme Court's restatement of the TSM test. KSR Int'l Co., 127 S.Ct. at 1739. In any event, as the Supreme Court suggests, a flexible approach to the TSM test prevents hindsight and focuses on evidence before the time of invention, see, e.g., In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998), without unduly constraining the breadth of knowledge available to one of ordinary skill in the art during the obviousness analysis.

This court finds that the claims of the '666 patent were unpatentable under 35 U.S.C. § 103(a). Gorai is within the scope of the relevant prior art because it both predates the '666 patent filing date of March 15, 1991 and discloses series 2-input multiplexer circuits. See Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1535 (Fed. Cir. 1983). Moreover a person of ordinary skill in the art would

have a thorough understanding of electrical switching systems and knowledge of actual electrical implementations of multiplexers such as the TGMs in Weste.

Specifically, the Gorai reference uses serial connectivity of 2:1 multiplexers, each described as M(1), to realize logic functions. The subject matter of the Gorai reference explains an approach (i.e., algorithm) to analyze mathematical dependencies among desired inputs and then selects appropriate input connections as well as series connectivity between M(1) multiplexers to realize the specified logic function. For example, the Gorai algorithm could result in the circuit in Fig. 6 defined by logic function:

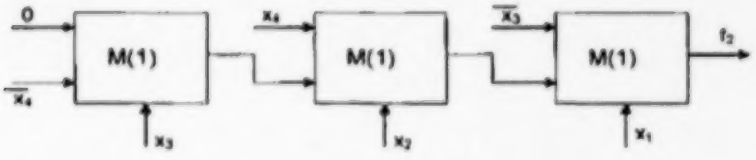


Fig. 6 Cascade network of f_2

In this appeal, Translogic proffers two arguments to attempt to show that the Gorai reference is not prior art with respect to the '666 patent. Initially, Translogic contends that neither the Gorai algorithm nor its circuit realizations provide a multiplexer function. In fact, since the entire point of Gorai's article revolves around logic, not multiplexing, with series connectivity among M(1) circuits, Translogic contends that Gorai teaches away from multiplexers. Next, Translogic contends that the Gorai reference discloses an algorithm

capable of providing designs for a large number of circuits, while the inventor of the '666 patent was modifying one circuit, a multiplexer, with utmost regard for its performance. In other words, while Gorai discloses an algorithm to design logic circuits based on functional parameters, the '666 patent improves a known circuit. In sum, Translogic's argument tries to state that the Gorai reference is not relevant prior art because the reference does not specifically disclose a N:1 series multiplexer but only discloses an algorithm to realize logic functions by using 2:1 multiplexers connected in series.

In its prior art argument, Translogic is making the same error corrected by the Supreme Court in KSR. Translogic mistakenly argues that variants of a circuit connecting 2:1 multiplexers in series are not relevant prior art with respect to the '666 patent because these variants do not address the same problem, namely an improved multiplexer circuit. However, this argument overlooks the fundamental proposition that the series circuits in Gorai are prior art within the public domain and the common knowledge of a person of ordinary skill in the art. Thus, the Gorai reference is a relevant prior art reference with respect to the '666 patent and clearly discloses a series 2:1 multiplexer circuit.

Translogic also puts forth a prior art argument based on the circuit inputs. Translogic contends that Fig. 3 in Gorai (see below) is a half-bare, incomplete circuit because all h and g inputs are undefined (variables or constants) and therefore the Fig. 3 circuit only shows three control inputs (x1, xp-1 and xp).

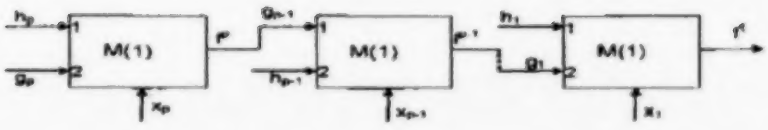


Fig. 3. A cascade network of p-stages of M(1)s

Therefore, Translogic states that the Gorai Fig. 3 circuit cannot be a multiplexer because the inputs are not specifically defined to realize a N:1 series multiplexer circuit (4:1 in this example).

Translogic's input argument is without merit. Claims 47 and 48 of the '666 patent define a series multiplexer circuit. Gorai Fig. 3 discloses the same serial multiplexer circuit. As any person of ordinary skill in the art would understand, the inputs to a circuit do not change the circuit itself. Therefore, this court finds that Gorai discloses a series multiplexer circuit as claimed in the '666 patent. Thus, the Board was correct in concluding that the Gorai reference discloses a series multiplexer circuit.

Lastly, Translogic contends that Gorai does not teach or suggest the use of TGMs for each M(1) stage (i.e., 2:1 multiplexer). Translogic admits that the Weste reference does disclose a TGM circuit; however, Translogic argues that Weste provides no specific teaching, suggestion or motivation to use TGMs in a series circuit such as shown in Gorai Fig. 3. Furthermore, Translogic notes that Weste discloses a TGM used for a single multiplexer but does not include any reference to coupled TGMs in series. Thus, according to Translogic, the Weste reference does not provide the necessary teaching,

suggestion or motivation to combine the use of TGMs with the Gorai reference.

As articulated by the Supreme Court in KSR an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." 550 U.S. at ---, 127 S.Ct. at 1741. In this case, a person of ordinary skill in the art at the time of the invention would have recognized the value of using a known element, a 2:1 TGM, as taught by Weste, for the 2:1 multiplexers in the series arrangement of multiplexers in Gorai. A person of ordinary skill in the art would have appreciated that any conventional multiplexer circuit could be utilized to implement the 2:1 multiplexer circuits in Gorai. After all, TGMs were well-known multiplexer circuits as evidenced by the Weste 1985 textbook. In other words, in looking for a multiplexer circuit for the individual 2:1 multiplexers disclosed in Gorai, a person of ordinary skill in the art would have solved this design need by "pursu[ing] known options within his or her technical grasp." Id. at 1742. Thus, this court agrees with the Board's determination. The Board based its decision on sound reasoning that a person of ordinary skill in the art would select a specific circuit based on the need for a 2:1 multiplexer circuit for the individual multiplexers shown in Gorai. Specifically, a person of ordinary skill in the art at the time of the invention would have been able to choose TGMs as an option. While other circuits could have been used to implement the 2:1 multiplexers, TGMs were a well-known circuit as

shown by the explanation of TGM circuits in the 1985 textbook by Weste. This court finds that substantial evidence in the record supports the Board's finding that a person of ordinary skill in the art would have used TGMs in the N:1 circuit configuration shown in Gorai. In sum, this court agrees with the Board's conclusion that the '666 patent is unpatentable under 35 U.S.C. § 103(a) over Gorai in view of Weste.

Because this court finds that Gorai in view of Weste renders the '666 patent unpatentable, the court will not address Tosser in view of Weste. However, the analysis of Tosser in view of Weste would undoubtedly reach the same result because Tosser also discloses a series multiplexer circuit.

IV

The decision of the Board, sustaining the final rejection of claims 16, 17, 39-45, 47 and 48 as obvious, is affirmed.

AFFIRMED

APPENDIX L

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 103

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED

OCT 26 2005

U.S. PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte TRANSLOGIC TECHNOLOGY INC.

Appeal No. 2005-1050
Reexamination Control Nos. 90/005, 384,
90/005, 823, 90/005, 881, 90/006, 051
and 90/006, 392

HEARD: May 31, 2005

Before KRASS, BARRETT, and NAPPI,
Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON REQUEST FOR REHEARING

Appellant filed a Request for Rehearing Under 37 C.F.R. § 41.52 on September 13, 2005, for rehearing of our original decision entered July 14, 2005.

The request for rehearing has been considered but is denied with respect to making any modifications in our decision.

ERRATUM

In our original decision, the page numbers in Appendix B mistakenly start with page 2. There is no page 1 in Appendix B.

ABBREVIATIONS

Pages of the request for rehearing are referred to as "RR___." Pages of the original decision are referred to as "D___." Pages of the brief and reply brief to the Board are referred to as "BR___" and "RBr___," respectively. Pages of the examiner's answer are referred to as "EA___."

DISCUSSION

Patent owner Translogic Technology, Inc. (TTI) argues that our decision raises new grounds of rejection for three reasons: (1) it introduces a new claim construction to which patent owner has no opportunity to respond; (2) it introduces new factual assertions concerning complex technology; and (3) it proposes a new ground of rejection using the Toshiba MUX8 reference (RR2). "TTI requests a full opportunity to address the new claim construction, the new factual assertions, and the new ground of rejection in the customary manner - in examination, so that these reexaminations can be brought to a timely conclusion." (RR5.) Thus, although not expressly stated, patent owner seeks for us to denominate our decision as containing a new ground of rejection under 37 C.F.R. § 41.50(b) (2004) so that

prosecution may be reopened before the examiner under § 41.50(b)(1).[1]

When an examiner rejects a claim as failing to meet one or more of the statutory requirements for patentability, procedural due process and 35 U.S.C. § 132 of the patent statute require that applicants be adequately notified of the reasons for the rejection of claims so that they can decide how to proceed. See In re Ludtke, 441 F.2d 660, 662, 169 USPQ 563, 565 (CCPA 1971). See also In re De Blauwe, 736 F.2d 699, 706, 222 USPQ 191, 197 (Fed. Cir. 1984) (remanding case to Patent and Trademark Office (PTO) because of failure to notify appellants that there was no objective evidence to support appellants' arguments). A patent applicant must have the opportunity to respond to new grounds for claim rejections put forth by the Board of Patent Appeals and Interferences (Board). See In re Waymouth, 486 F.2d 1058, 1061, 179 USPQ 627, 629 (CCPA 1973) ("To attempt to deny appellants an opportunity to provide a different and appropriate response to the board's [new] rejection ... does not satisfy the administrative due process established by Rule 196(b) of the Patent Office."). Rule 196(b) refers to 37 C.F.R. § 1.196(b), superseded by 37 C.F.R. § 41.50(b) (2004). A new rejection may occur

---

[1] Although § 41.50(b) also permits an appellant the option of arguing the merits of a new ground of rejection in a request for rehearing, § 41.50(b)(2), since patent owner has not argued the merits of the alleged new grounds of rejection in the request for rehearing we presume it would elect further prosecution before the patent examiner.

where the examiner and board reject a claim for different reasons. Waymouth, 486 F.2d at 1060-61, 179 USPQ at 629 (new ground of rejection where "the bases of [the examiner's and Board's] rejection were wholly different, necessitating different responses by appellants."). The Board's new findings and reasons must be material to the rejection to create a new ground of rejection. See In re Kumar, 418 F.3d 1361, 1368, 76 USPQ2d 1048, 1052 (Fed. Cir. 2005) ("When a rejection for obviousness is based on overlapping values in the prior art, identification of the values deemed to overlap is material to the rejection. In this case the overlapping values were identified for the first time in the decision of the Board, and are not themselves set forth in Rostoker or any other reference. In calculating the overlapping values, the Board found facts not found by the examiner regarding differences between the prior art and the claimed invention, which in fairness required an opportunity for response."). A rejection is not based on new grounds if "appellants have had fair opportunity to react to the thrust of the rejection." In re Kronig, 539 F.2d 1300, 1302, 190 USPQ 425, 426 (CCPA 1976); id. at 1303, 190 USPQ at 427 (finding that an applicant had fair opportunity to challenge a rejection because "[t]he basic thrust of the rejection at the examiner and board level was the same").

We have considered patent owner's arguments, but are not persuaded that our decision presented any new grounds of rejection. Accordingly, we will not denominate our decision as containing a new ground of rejection under 37 C.F.R. § 41.50(b) or otherwise modify our original decision.

(1) Claim interpretation

Patent owner argues that "[t]he decision introduces a claim construction that differs from the claim construction adopted by the Examiner" (RR2) and "[b]y newly construing the claims, the Decision effectively offers a new series of rejections, without providing opportunity to argue, amend or cancel claims, or submit evidence in view of this new claim construction" (RR3).

A new ground of rejection, by definition, is a rejection which is new to the appellant. It is not a new ground of rejection where an appellant and the examiner expressly argue different claim interpretations and the Board sides with the appellant or the examiner because in that case the appellant has actually argued the claim interpretation. Thus, where the Board adopts the patent owner's argued claim interpretation, it is not a new ground of rejection even though the interpretation is different from the examiner's interpretation. It should also go without saying that a claim interpretation that is not material to the rejection does not raise a new ground of rejection. Patent owner alleges that certain claim interpretations are new or different from those stated by the examiner without mentioning that it addressed the claim interpretations in its briefs to the Board and without attempting to show how the claim interpretation affects the rejection to create a new rejection.

(i)

Patent owner argues that "for the first time, a construction of 'coupled to receive' is offered. Decision at 11." (RR2).

This is not a new claim interpretation. The claim interpretation issue in the limitations of a "signal input terminal coupled to receive [first, second, third, fourth, or fifth] input variable" and a "control input terminal coupled to receive a [first, second, third, or fourth] control signal" is whether the terminals must be actually coupled to input variables or control signals or just capable of receiving these signals, i.e., whether the input variables and control signals are part of the claimed combination. The examiner concluded that the "input signals cannot be relied upon to patentably distinguish the claims over the combined prior art because the claims are directed to an apparatus, and the input signals are not part of this apparatus (i.e., they are merely intended use)" (EA10-11). Patent owner expressly agreed with this interpretation (repeating the quoted language and stating "Patentee agrees" (RBrl4)) and, so, responded to the examiner's interpretation. Therefore, our claim interpretation is not new, but just memorializes this agreed upon interpretation that the limitation of a "signal input terminal coupled to receive [first, second, third, fourth, or fifth] input variable" refers to the structure of a "[t]erminal capable of receiving an input variable" (D11). "That is, the 'input variable' itself is not part of the claimed combination and these limitations are anticipated by an input terminal structure without it having to be actually connected to an input variable signal." (D11.) Similarly, the limitation of a "control input terminal

coupled to receive a [first, second, third, or fourth] control signal" refers to a "[t]erminal capable of receiving a control signal. The control signal itself is not part of the claimed structure." (D10.) This is not a new claim interpretation and does not present a new ground of rejection.

(ii)

Patent owner argues (RR2):

> [T]he Decision construes first, second, and third control signals to be independent and unique. Decision at 10. In contrast the Examiner's Answer states that the claims do not recite three different control signals. Examiner's Answer at 10.

To explain the claim interpretation issue, we begin with the arguments. In the brief, patent owner argued (Br11):

> The claimed 4:1 multiplexer circuits have three stages with four signal input terminals and terminals and three control input terminals coupled to receive four different input variables and three different control signals, respectively. The claimed 5:1 multiplexer circuits have four stages with five signal input terminals and four control input terminals coupled to receive five different input variables and four different control signals, respectively.

The examiner correctly stated that "nowhere do the claims recite 'four different input variables', 'three

different control signals', etc." (emphasis added) (EA10), but "that even if such terminology were set forth in the appealed claims, the obviousness rejection based on Gorai would still be proper, as all of the input variables and control inputs of the Fig. 3 circuit are indeed different from each other" (EA10).

Our claim interpretation stated that the claimed first, second, third, fourth, and fifth "input variables" do not require five different input variables, or that the "input variables" are different from the first, second, third, and fourth "control signals" (D11-12). We further stated that "[i]n any case, since the input variables are not part of the claimed structure, the nature of the input variables is not a positive claim limitation" (D12). This claim interpretation is not contested.

The examiner correctly interpreted the claims to not expressly require the first, second, third, and fourth "control signals" to be different. We stated (D10): "In a multiplexer circuit, these control signals are unique and independent of each other. However, the actual control signals are not part of the claimed multiplexer structure." Thus, we found that the control signals in a multiplexer are inherently different from each other even though not expressly recited in the claims. There are several reasons why this is not a new ground of rejection. First, the "control signals" are not part of the claimed multiplexer structure (D10), and the control input terminal only needs to be "capable of receiving a control signal" (Dl0), so the interpretation that the control signals are independent of each other does not affect the rejection and does not raise a new

ground of rejection. Second, the claim interpretation is in patent owner's favor and does not require any argument or amendment to rebut, so it is difficult to see how patent owner can reasonably consider it to be a new ground of rejection requiring reopening of prosecution. Third, the claim interpretation is consistent with patent owner's express arguments that the claims require different "input variables" and "control variables" (see discussion of argument (3), D50-62), so it is not a new ground of rejection to patent owner. Fourth, the examiner noted that even if the word "different" was in the claims, Fig. 3 of Gorai teaches "different" control signals and input variables and, therefore, the examiner's rejection addressed the claim interpretation argued by patent owner. This claim interpretation does not present a new ground of rejection.

(iii)

Patent owner argues (RR2-3):

The Decision further states that a variable and its logical complements are the same variable. Decision at 68. In contrast, the Examiner's Answer states that a variable and its logical complement are different variables. Examiner's Answer at 9 (stating that D and /D are first and second input variables).

Our decision agreed with patent owner's statement that a variable and its logical complement are the same variable. More precisely, we stated that a variable and its complement represent different states of the same variable (D68) since a variable and its complement are not the same thing. Since patent owner expressly argued the

interpretation of "variable," the claim interpretation is not a new ground of rejection to patent owner.

Furthermore, the examiner did not interpret a variable and its logical complement to be the same variable, so our interpretation is not inconsistent with the examiner's. What the examiner actually stated was that "[first and second input variables D and /D are applied to the inputs of a first 2:1 multiplexer stage" (EA9), which patent owner argues to be a statement that a variable and its complement are the same variable. Patent owner's argument that the examiner interpreted a variable and its complement to be the same logical variable is only true if one reads in an implied limitation that the first, second, third, and fourth input variables in claim 47 are different, and then reasons that because the D and /D (D complement, also written as $\overline{D}$) represent the same variable, they cannot be first and second different input variables. As noted in Section (1)(ii), supra, the examiner correctly concluded that the claims do not require the input variables to be different from each other (EA10) and we agreed with that claim interpretation (D11-12). Since the claims do not require the input variables to be different, the examiner merely stated that the first and second input variables were D and /D, not that D and /D are the same variable as argued by patent owner.

Still another reason why our statement that a variable and its logical complement represent different states of the same variable does not raise a new ground of rejection is because the "input variables" and the "control signals" are not part of the claimed combination and do not affect the

rejection. Patent owner agrees that the "input variables" and "control signals" are not part of the claimed combination and the limitations of a "signal input terminal coupled to receive [first, second, third, fourth, or fifth] input variable" and a "control input terminal coupled to receive a [first, second, third, or fourth] control signal" are met by terminals capable of receiving these input variables and control signals (D11; D10). The examiner's rejection expressly found that Gorai and Tosser have terminals capable of receiving input variables and control signals.

(iv)

Patent owner argues (RR3):

> The Decision also adopts a new construction of the term "input variable." According to the Decision, a variable "must be capable of assuming, at any given time, either one of at least two values." Decision at 10 (citing Claim Construction attached to the Order of May 12, 2005 in Translogic Technology Inc. v. Hitachi. Ltd.). In contrast, the Examiner's Answer states that all input signals are "'input variables' regardless of whether they are set to a constant value." Examiner's Answer at 15.

Patent owner argued the constant inputs (0, 1) to the three-stage cascade of Fig. 6 of Gorai "are constants, and thus cannot correspond to recited input variables" (Br14). The examiner responded (EA15-16):

> This argument is also without merit because clearly all of the nine input signals

> shown in Gorai's Fig. 3 can be interpreted as "input variables" (indeed it is the reason that Gorai uses alphanumeric designations for the different input signals). Moreover, these input signals are all "input variables" regardless of whether or not they are set to a constant value, or set to time-varying values (again note that the claims are being construed using the broadest reasonable interpretation test). The argument that an "input variable" cannot be a constant value is not correct (as just one example, note the well-known equation F=ma, where the terms can of course be interpreted as "input variables" even when they are equal to constant values).

Patent owner argued that the examiner errs in stating that input signals are all "input variables" regardless of whether or not they are set to a constant value because a constant (0 or 1) is not a variable (RBr16-17).

The examiner properly found that Fig. 3 of Gorai teaches that all multiplexer inputs can be "variables." This is the rejection to be reviewed. Our decision agreed with patent owner that a constant (0 or 1) is not a variable and stated that "[a] variable must be capable of assuming, at any given time, either one of at least two values (0 or 1), whereas a constant has a fixed value" (D69), although we noted that the examiner's statement that a constant could be considered an input variable is not without support (D10-11). Since patent owner expressly argued the claim interpretation, our agreement with patent owner's claim interpretation does not raise a

new ground of rejection to patent owner. In addition, our decision stated that "since the input signals are not part of the claimed structure, it does not matter whether the inputs are variables or constant as long as the multiplexer is capable of handling variables" (D70), so the claim interpretation does not affect the rejection and does raise a new ground of rejection. The rejection is based on the finding that the structures in Gorai and Tosser are capable of receiving variables at their input terminals. This claim interpretation does not present a new ground of rejection.

(v)

Patent owner argues (RR3):

> Based on this new claim construction, the Decision notes (in additional comments) that all pending claims may be unpatentable in view of the conventional multiplexer circuit shown in the Toshiba TC19G000 Series, MUX8 Macrocell Data Sheet (the Toshiba MUX8 reference). Decision at 76-78. The Toshiba MUX8 circuit is described in the background section of the '666 patent at col. 1, lines 27-34, and the claimed multiplexer circuits are specifically distinguished from such a conventional multiplexer at col. 2, lines 3-7. A claim construction that captures prior art specifically distinguished in the patent is manifestly unreasonable. Whether the construction proposed in the Decision mandates such an unreasonable result should be decided, not merely flagged as a possibility, as it would either be grounds to change the

construction, or a new ground of rejection which should be remanded for further action by the examiner and response by the patentee.

As discussed in Section (3), infra, the additional comments of APJ Barrett are not the decision of the Board and, therefore, do not raise a new ground of rejection. Accordingly, the arguments regarding the Toshiba MUX8 are not considered.

(2) Factual assertions

Patent owner argues (RR3-4):

The Decision includes extensive assertions concerning various aspects of logic design such as those provided at, for example, Appendices B-C. The Decision attempts to support these assertions by, for example, stating that they are "self-evident to any computer scientist or electrical engineer who has taken an undergraduate computer science course in switching theory and the design of digital logic circuit." Decision at B-2. The Decision thus apparently relies either on the Panel's own technical background or the taking of Official Notice for such assertions. Both are improper. While the U.S. Patent and Trademark Office (PTO) is accorded expertise in patent examination, the PTO is not deemed to have expertise in technology. Sandvik Aktiebolag v. Samuels, [not reported in F. Supp, 1991 WL 25774], 20 USPQ 1879 at 1880 (D.D.C. 1991) (noting the Commissioner's need for "true experts"). Official Notice is also improper. "Official Notice unsupported by documentation

> should be taken only ... where the facts asserted to be well-known ... are capable of instant and unquestionable demonstration." MPEP, 8th Ed. § 2144.03 at 2100-136. In addition, "technical facts in the areas of esoteric technology ... must always be supported by citation to some reference work." Id. (citing In re Ahlert and Kruger, 424 F.2d at 1091, 165 USPQ 418 at 420-21 (C.C.P.A. 1970)). Even if introduction of these factual assertions were proper, Patentee has no opportunity to respond.

The appendices A-C merely provide technical background to aid the reader's understanding of the Gorai and Tosser references and do not add any facts or reasons that are necessary to or relied upon in the rejection. For example, Appendix A explains what is meant by Gorai's statement that "an M(p) can realize any function of (p+1) variables" (page 164) to provide a complete technical answer to appellant's erroneous argument that the statement means that a series of 2:1 multiplexers with p control input inputs can realize functions of at most (p+1) variables (D15-16; D54). However, Appendix A is not necessary to or relied upon in the rejection itself. Appendix B provides a definition of terminology used in Gorai and Tosser and is not necessary to or relied upon in the rejection. If the reader prefers to rely on her or his own knowledge or research to determine what is meant, she or he is free to do so. Appendix C explains how the examples in Gorai use multiplexers to realize logic functions and is not necessary to or relied upon in the rejection. We could have left it to the reader's knowledge or ability to find out or

develop this background information himself or herself, but since we are aware that most judges do not have technical backgrounds in computer science and the design of digital logic circuits, we thought a background explanation would be helpful. The addition of explanatory background material does not change the rejection and does not raise a new ground of rejection.

As to patent owner's argument that "[w]hile the U.S. Patent and Trademark Office (PTO) is accorded expertise in patent examination, the PTO is not deemed to have expertise in technology" (RR4), we note that Judge Oberdorfer said the "while patent examiners are experts in reviewing patent applications in particular fields, they do not have actual experience in the technology," Sandvik v. Samuels, 1991 WL 25774, 20 USPQ2d at 1880. Thus, Judge Oberdorfer stated that examiner are experts in their particular fields, but not have "actual experience": he did not say that examiners do not have "expertise". Also, "administrative patent judges shall be persons of competent legal knowledge and scientific ability." 35 U.S.C. § 6(a). Although the Director retains outside experts (at plaintiff's expense) in civil actions under 35 U.S.C. § 145, this does not imply that the Board lacks technical expertise. In any case, the appendices merely provide technical expertise. In any case, the appendices merely provide technical background and are not relied upon in the rejections, so they do not raise a new ground of rejection.

As to patent owner's arguments about Official Notice, this is not a situation where the Board has

relied upon Official Notice for some fact relied upon in the rejection. The examiner's rejection is not changed in any way by the appendices and they do not raise a new ground of rejection.

(3) Additional comments in the decision

Appellant argues that the additional remarks to the decision introduce a new ground of rejection (RR4):

> According to additional remarks in the Decision, the conventional multiplexer circuit shown in the Toshiba MUX8 reference that was considered in the original prosecution of the '666 patent renders all pending claims unpatentable. The additional remarks note that the Panel did not "want to raise any new question of a new ground of rejection in the main opinion." Decision at 76. As best understood by patentee, according to the Panel, all pending claims may be unpatentable in view of the Toshiba MUX8 reference with at least one Panel member concluding that they are unpatentable. If this is a potential new ground of rejection it should be fully addressed whether or not the Panel "wants" to raise it. If this is not a new ground of rejection, then, according to the Panel as a whole, all pending claims are patentable in view of the Toshiba MUX8 reference, and any subsequent request for reexamination based on the Toshiba MUX8 reference would not raise a substantial new question of patentability, and would not be granted. In any case, introduction of this

"new" ground of rejection at this stage of examination effectively denies TTI the opportunity to respond. The issue should be decided after full examination, not merely flagged for possible future action after the patentee prevails on appeal.

The additional comments of APJ Barrett (D76-78) do not constitute the decision of the Board, just as a dissenting or concurring opinion by an appeals court judge does not represent the decision of the court. Therefore, the additional comments of APJ Barrett do not raise ground of rejection and are not subject to judicial review. The opinion was modeled after SSIH Equip., S.A. v. United States Int'l. Trade Comm'n, 718 F.2d 365, 218 USPQ 678 (Fed. Cir. 1983) (Nies, J., authoring the opinion and providing additional comments). Two APJs agree with the opinion up to the page with their signatures: this is the decision of the Board that is subject to judicial review. APJ Barrett agrees with the first portion of the opinion (since he authored it) and expresses additional views. The additional views of one APJ that a rejection would be appropriate does not constitute a new ground of rejection because one APJ alone cannot enter a new ground of rejection. The Board is not required to raise all potential new grounds of rejection, especially where, as here, the examiner's rejections are affirmed. The fact that the additional comments do not constitute a new ground of rejection does not in any way imply that the claims are patentable over the Toshiba MUX8 reference.

CONCLUSION

Patent owner's request for rehearing has been considered, but we are not persuaded that our decision presented any new grounds of rejection. Accordingly, the request for rehearing is denied with respect to making any modifications in our decision or denominating our decision as containing a new ground of rejection under 37 C.F.R. § 41.50(b).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). See 37 C.F.R. § 1.136(a)(1) (iv).

DENIED

s/Errol A. Krass
ERROL A. KRASS
Administrative Patent Judge

s/Lee E. Barrett
LEE E. BARRETT
Administrative Patent Judge

s/Robert Nappi
ROBERT E. NAPPI
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

KLARQUIST SPARKMAN, LLP 121 SW SALMON STREET SUITE 1600 PORTLAND, OR 97204	Attorney for Patent Owner
ALAN R. LOUDERMILK LOUDERMILK & ASSOCIATES P.O. BOX 3607 LOS ALTOS, CA 94024-0607	Third Party Requester

APPENDIX M

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 100

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED

JUL 14 2005

U.S. PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte TRANSLOGIC TECHNOLOGY, INC.

Appeal No. 2005-1050

Reexamination Control Nos. 90/005,384,

90/005,823, 90/005,881, 90/006,051,

and 90/006,392

HEARD: May 31, 2005

Before KRASS, BARRETT, and NAPPI, Administrative Patent Judges,

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. §§ 306 and 134(b) from the final rejection of claims 16, 17, 39-45, 47, and 48, all of the pending claims. Patent claims 1-15 and 18-27 have been canceled and claims 28-38 and 46 added during the reexaminations have been canceled.

We affirm.

REEXAMINATIONS

This appeal involves five merged reexamination proceedings for reexamination of U.S. Patent 5,162,666 ('666 patent), entitled "Transmission Gate Series Multiplexer," issued November 10, 1992, to Dzung J. Tran, based on application 07/670,075, filed March 15, 1991, now assigned to Translogic Technology, Inc., 7353 S.E. Hacienda, Hillsboro, Oregon, 97123.

Reexamination Control No. 90/005,384 was filed June 4, 1999, by a third party requester, Alan R. Loudermilk.

Reexamination Control No. 90/005,823 was filed September 26, 2000, by third party requester Alan R. Loudermilk and merged with the first reexamination proceeding.

Reexamination Control No. 90/005,881 was filed December 8, 2000, by third party requester Alan R. Loudermilk and merged with the first two reexamination proceedings.

Reexamination Control No. 90/006,051 was filed July 3, 2001, by the patent owner, Translogic Technology, Inc. (TTI), and merged with the first three reexamination proceedings.

Reexamination Control No. 90/006,392 was filed September 27, 2002, by third party requester Alan R. Loudermilk and merged with the first four reexamination proceedings.

RELATED LITIGATION

The '666 patent is the subject of Translogic Technology Inc. v. Hitachi, Ltd., No. 99-407-PA (D. Ore. filed March 24, 1999). A jury verdict was signed on October 27, 2003, and entered on October 29, 2003, determining that Hitachi had not proved by clear and convincing evidence that claims 16 and 17 of the '666 patent were invalid for anticipation or obviousness. On February 22, 2005, the district court adopted a special master's report and recommendation on infringement finding infringement of claims 16 and 17 of the '666 patent and granted plaintiff's motion for summary judgment of infringement. A jury verdict was signed on May 6, 2005, and entered on May 10, 2005, finding inducement of infringement of claims 16 and 17, and awarding damages of $86.5 million. An order granting plaintiff's motion for a permanent injunction and denying defendant's motion for a stay was signed on May 12, 2005, and entered on May 13, 2005. A notice of appeal and an emergency motion for stay of the permanent injunction pending appeal were filed in the U.S. Court of Appeals for the Federal Circuit on May 12, 2005.

BACKGROUND

The invention relates to a type of digital logic circuit known as a "multiplexer," or "MUX" for short. A multiplexer circuit has one or more control inputs that control the device to select one of several data inputs to connect to a single output line. A conventional k:1 multiplexer with p control lines selects one of $k=2^p$ data input lines to connect to a

single output line; e.g., a 2:1 multiplexer has one control input and two data inputs, a 4:1 multiplexer has two control inputs and four data inputs, etc.

The claims on appeal are directed to a multiplexer having three or four 2:1 transmission gate multiplexers (TGMs) connected in series, that is, with the output of a TGM connected to one input of the next TGM. Each TGM in the series is called a "stage." A TGM is constructed using transmission gates (TGs), which are electronic circuits that pass the input (a logical "0" or "1") to the output when the control input is a logical "1" and block the input when the control input is a logical "0." A multiplexer constructed from a series of TGMs has p control inputs and $(p+1)$ data inputs for total of $(2p+1)$ inputs; thus, a series 4:1 multiplexer has $p=3$ control inputs instead of 2 control inputs as in a conventional multiplexer.

Representative claims 47 is reproduced below.

47. A multiplexer circuit comprising:

a first stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

the first and second signal input terminals coupled to receive first and second input variables, respectively;

the control input coupled to receive a first control signal;

a second stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the second stage input terminals coupled to the first stage output terminal;

the other one of the second stage input terminals coupled to receive a third input variable;

the second stage control input terminal coupled to receive a second control signal;

a third stage TGM circuit having first and second signal input terminals, a control input terminal and an output terminal;

one of the third stage input terminals coupled to the second stage output terminal;

the other one of the third stage input terminals coupled to receive a fourth input variable; and

the third stage control input terminal coupled to receive a third control signal;

whereby the circuit forms a 4:1 multiplexer.

THE REFERENCES

The examiner relies on the following references:

Tosser, A.J., and Aoulad-Syad, D. ("Tosser"), Cascade networks of logic functions built in multiplexer units, IEE Proc., Vol. 127, Pt. E, No. 2, March 1980, pages-64-68.

Weste, Neil H.E., and Eshraghian, Kamran ("Weste"), Principles of CMOS VLSI Design: A Systems Perspective (1985 Addison-Wesley Publ. Co.), pages 14-17 and 172-175.

Gorai, R.K., and Pal, A. ("Gorai"), Automated synthesis of combinational circuits by cascade networks of multiplexers, IEEE Proc., Vol. 137, Pt. E, No. 2, March 1990, pages 164-170.

THE REJECTIONS

Pages of the final rejection are referred to as "FR__" and pages of the examiner's answer are referred to as "EA__." Pages of the appeal brief are referred to as "Br__" and pages of the reply brief are referred to as "RBr__."

Claims 16, 17, 39-45, 47, and 48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gorai and Weste. The examiner finds that Fig. 3 of Gorai teaches a three-stage multiplexer with four input signals (h_p, g_p, h_{p-1}, h_1) and three control signals (x_p, x_{p-1}, and x_1) (FR2). The examiner finds that Gorai does not disclose that the multiplexers are transmission gate multiplexers (TGMs) (FR2-3). The examiner finds that Weste teaches 2:1 TGM circuits which transfer full logic "0" or "1" signals between the input and output (FR3). The examiner concludes that one of ordinary skill in the art would have been motivated to use the TGM circuit in Weste for the

multiplexers in Gorai for this reason (FR3). The examiner also finds that the fact that Gorai only shows "black boxes" for the multiplexer stages would have suggested to one skilled in the art to use any conventional multiplexer circuit, such as the TGM taught by Weste (FR3-4). The examiner finds that Fig. 3 of Gorai is a network of *p* stages, which suggests any number of cascaded multiplexers, including the 4-stage multiplexer of claim 48 (FR4).

Claims 16, 17, 39-45, 47, and 48 stand rejected under 35 U.S.C. §.103(a) as being unpatentable over Tosser and Weste. The examiner finds that Fig. 9 of Tosser teaches a 4:1 multiplexer having three cascaded 2:1 multiplexer stages (FR5). The examiner finds that Tosser does not disclose that multiplexers are implemented using TGMs (FR5). The examiner finds that Weste teaches 2:1 TGM circuits which transfer full logic "0" or "1" signals between the input and output (FRS). The examiner concludes that one of ordinary skill in the art would have been motivated to use the TGM circuit in Weste for the multiplexers in Tosser for this reason (FR5-6). The examiner also finds that the fact that Tosser only shows "black boxes" for the multiplexer stages would have suggested to one of ordinary skill in the art to use any conventional multiplexer circuit, such as the TGM taught by Weste (FR6). The examiner concludes that it would have been obvious to add an additional stage to the multiplexers to allow processing of more input signals (FR7).

OPINION

Grouping of claims

Patent owner states that claim 47 is representative of the 4:1 multiplexer claims 16, 39-41, 45, and 47, and that claim 48 is representative of the 5:1 multiplexer claims 17, 42-44, and 48 (Br11). This grouping of claims was confirmed at the oral hearing. Claims 47 and 48 correspond to original patent claims 16 and 17 in the '666 patent, rewritten in independent form, which were held not invalid and infringed in Translogic v. Hitachi. Thus, claims 16, 39-41, 45, and 47 stand or fall together with claim 47, and claims 17, 42-44, and 48 stand or fall together with claim 48.

Claim interpretation

The following is an interpretation of terms in claims 47 and 48. The interpretation is consistent with that in the claim construction attached to the Order of May 12, 2005, in Translogic v. Hitachi, except for the interpretations of "one of the fourth stage input terminals coupled to the third stage output terminal," and like limitations, which are unimportant to the analysis and the outcome. Several additional terms are defined.

TERM	INTERPRETATION
"multiplexer"	A circuit that accepts a plural number (N) of input signals and, based on the state of control signals that are received by the multiplexer, selects as an output a single one of the input signals.

TERM	INTERPRETATION
"comprising"	"'Comprising' is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim." Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1633 (Fed. Cir. 1997).
"TGM" or "TGM circuit"	A 2:1 multiplexer comprising a pair of transmission gates together with their associated control input and inverter, with the outputs of the transmission gates connected together ('666 patent, col. 2, lines 63-66). Each of the transmission gates may consist of a single pass transistor or a complementary pair of transistors ('666 patent, col. 1, lines 46-50).
"control signal"	A signal applied to a TGM control input terminal that controls

TERM	INTERPRETATION
	the TGM to select one of the two input terminals for connection to the output terminal. This construction does not preclude the control signal from being used to control another TGM outside of the claimed multiplexer. Compare claim 42 (not argued) which recites "wherein TGM circuit loading on the first control signal consists of a single TGM circuit," which precludes applying the control signal to another TGM.
first, second, third, and fourth "control signals"	In a multiplexer circuit, these control signals are unique and independent of each other. However, the actual control signals are not part of the claimed multiplexer structure.
signal input terminal "coupled to" a previous stage output terminal	Connected to, directly or through one or more intervening inverters or buffers.
control input terminal "coupled to receive" a control	Terminal capable of receiving a control signal. The control signal itself

TERM	INTERPRETATION
signal	is not part of the claimed structure.
"input variable"	A signal to be input to one of the input terminals of a TGM. Patent owner agrees that the "input variable" itself is not part of the claimed structure (RBr14). A "variable" is defined as: "A symbol used to represent an unspecified member of some set. A variable is a 'place holder' or a 'blank' for the name of some member of the set. Any member of the set is a value of the variable and the set itself is the range of the variable. If the set has only one member, the variable is a constant." James and James, Mathematics Dictionary (5th ed. Chapman & Hall 1992). A "variable" is also defined as: "1: something that is variable 2 a: a quantity that may assume any one of a set of values b: symbol representing a

TERM	INTERPRETATION
	variable." Webster's New Collegiate Dictionary (G.&C. Merriam Co. 1977). Thus, a "variable" does not necessarily imply a variation in value over time. The district court's interpretation is that a variable "must be capable of assuming, at any given time, either one of at least two values." Claim construction attached to Order of May 12, 2005, in Translogic v. Hitachi. The definitions provide some support for the examiner's position (at EA16) that a variable can have a constant value, e.g., when the variable in an expression is solved for a constant value. However, we adopt the district court's interpretation because it is more consistent with the dictionary definition of a quantity that may assume one of a set of values.

TERM	INTERPRETATION
signal input terminal "coupled to receive" an input variable	Terminal capable of receiving an input variable. Patent owner agrees (RBr14) with the examiner's interpretation that the "input signals cannot be relied upon to patentably distinguish the claims over the combined prior art because the claims are directed to an apparatus, and the input signals are not part of this apparatus (i.e., they are merely intended use)" (EA10-11). That is, the "input variable" itself is not part of the claimed combination and these limitations are anticipated by an input terminal structure without it having to be actually connected to an input variable signal.
"having"	An open ended term, like "comprising." Therefore, the limitations defining the various stage TGM circuits do not exclude additional elements.

TERM	INTERPRETATION
first, second, third, fourth, and fifth "input variables"	As noted above, patent owner agrees that the "input variables" are not part not part of the claimed structure (RBr14). However, patent owner argues that theme limitations require: (1) five independent input variables; (2) that the input variables are independent from the control signal variables; and (3) the input variables cannot be constants (0 or 1). We interpret that these limitations: (1) require the signal input terminals to be "capable of" connecting to five different input variables (i.e., that there is a separate input terminal for each variable), but that the input variables applied to the terminals do not necessarily have to be independent or different; (2) do not preclude some of the input variables from being the same as some

TERM	INTERPRETATION
	of the control variables as long as there are separate input terminals for input variables and control signal variables; and (3) do not preclude the input signals from being constants as long as the multiplexer can accept variables.[1] A multiplexer selects one of the input variables as an output. It makes no difference to the multiplexing structure and operation whether the input variables are independent of each other or independent of the control variables, or whether the inputs are variables or constants. In any case, since the input variables are not

[1] For example, it was noted in the patent owner's response of November 20, 2000, with respect to Japanese Laid Open Patent Application No. H1-281529, to Goto, that when an input is always a constant "1" or "0," one element of the transmission gate may usually be omitted (referring to page 7 of the translation). Such a TGM would not be capable of handling a variable.

TERM	INTERPRETATION
	part of the claimed structure, the nature of the input variables is not a positive claim limitation. It also seems unlikely that patent owner would admit that a serial TGM structure which has control and input terminals capable of connecting to independent input and control variables would not infringe if it was connected so that some inputs were control variables and some inputs were constants. This goes to the use of the multiplexer structure, not the structure itself. "That which would literally infringe, if later in time, anticipates if earlier than the date of invention." Lewmar Marine, Inc. v. Barient, Inc., 827 F.2d 744, 747, 3 . USPQ2d 1766, 1768 (Fed. Cir. 1987).

TERM	INTERPRETATION
"one of the fourth stage input terminals coupled to the third stage output terminal"	The district court interpreted this limitation as follows: "This means that the third stage output terminal cannot also be coupled to other circuitry such that the overall result is not a N:1 multiplexer circuit." Claim construction attached to Order of May 12, 2005, in Translogic v. Hitachi. However, a multiplexer structure does not cease to become a multiplexer because of the way the intermediate and/or final TGM outputs are connected to surrounding external circuitry. Therefore, we interpret this limitation to not preclude coupling the third stage output terminal to other circuitry. This difference in interpretation plays no part in the decision.
"one of the third stage input terminals coupled to the second stage	See previous definition.

TERM	INTERPRETATION
output terminal" and "one of the second stage input terminals coupled to the first stage output terminal"	
"whereby ..."	"A 'whereby' clause that merely states the result of the limitations in the claim adds nothing to the patentability or substance of the claim." Texas Instruments, Inc. v. United States Int'l, Trade Comm' n, 988 F.2d 1165, 1172, 26 USPQ2d 1018, 1023 (Fed. Cir. 1993). Here the limitations "whereby the circuit forms a 4:1" (claim 47) and "whereby the circuit forms a 5:1 multiplexer" (claim 48) merely state the result of the structure and add no further limitation. Thus, we agree with the district court's interpretation that "[t]hese clauses are to be disregarded." Claim construction attached to Order of May

TERM	INTERPRETATION
	12, 2005, in Translogic v. Hitachi.

Factual findings

Scope and content of the prior art

Scope

Both Gorai and Tosser disclose serial 2-input multiplexer networks as in the claimed invention and, thus, are within the scope of the prior art. See Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1535, 218 USPQ 871, 876 (Fed. Cir. 1983) ("The scope of the prior art has been defined as that 'reasonably pertinent to the particular problem with which the inventor was involved'."). No issue of nonanalogous art has been raised.

Content

Gorai

Gorai discusses synthesis of combinational circuits using a cascade of 2-input multiplexer units (abstract). Although multiplexers were originally developed to perform the function of mulitplexing, i.e., selecting one of several inputs to connect to a single output line, they have also found widespread application as general-purpose logic devices because it has been shown "that multiplexers (MUX) can be used as universal logic modules in the realisation of combinational circuits" (page 164). A universal logic module of a specified number of variables is a circuit that can be used to implement any logic function up

to that number of variables by simply arranging its input/output terminal connections. The rejection relies on the background discussion of multiplexers and the cascade (serial) arrangement of 2-input (2:1) multiplexers in sections 1 and 2, and not the method of synthesizing combinational circuits described in sections 3-8.

A conventional multiplexer with k inputs, *p* control lines, and one output line is shown in Fig. 1 (page 164), shown below.

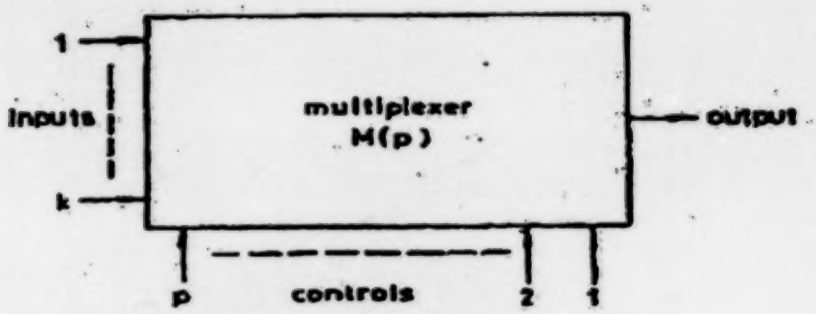


Fig. 1 *Block diagram of a multiplexer*

In a conventional multiplexer, *p* control lines select one of the $k=2^p$ inputs to output on the output line (id.). Gorai states that a conventional multiplexer with *p* control lines is designated as *M(p)* and "an *M(p)* can realize any function of (*p*+1) variables" (id.); e.g., an M(1) can realize any of the 16 possible functions of p+1=2 variables. It does not mean, as argued by patent owner, that an *M(p)* is limited to functions of only (*p*+1) variables; a technical explanation is provided in Appendix A. Gorai states (id.):

> Moreover, it may be noted that a *M(p)* having $p + k$ ($= p + 2^p$) inputs has the potential of realising functions of up to $(p + 2^p)$ variables. For example, let us compute the number of distinct functions realisable by *M*(3). Since there are 11 inputs [p=3 control lines plus $k=2^3=8$ inputs], it can realise functions of up to 11 variables. By connecting three variables to three control inputs, the remaining 8 variables, or their complements or constant (0 or 1) can be connected to each of the 8 input lines. So, there are 18 possible values [8 variables, 8 variable complements, plus two constants] for connecting to each of the 8 input lines resulting in $(18)^8$ distinct functions. Some more distinct functions can be realised by interchanging the control and input variables. Thus an *M*(3) can realise more than $(18)^8$ distinct functions of which less than one part of a million forms the functions of four [p+1=3+1=4] and lower variables. The rest are the functions of 5 to 11 variables. [Explanation in brackets added.]

Thus, a 2:1 multiplexer *M(1)* with p=1 control input and $k=2^1=2$ input variables can realize functions of up to $p+2^1=3$ variables (and can realize all functions of p+1=2 variables). Each non-control input may be one of two variables, one of two variable complements, or a constant (0 or 1) (6 possible inputs) for a total of $6^2=36$ possible functions of three variables.

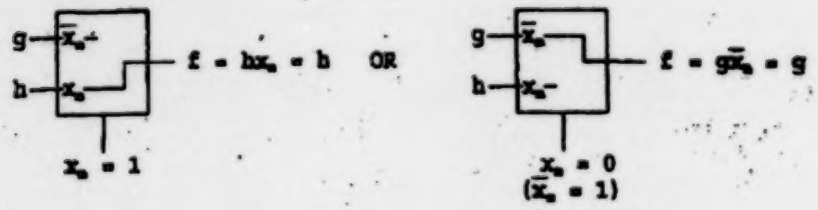
Gorai provides the general expression for an *M(1)* connected to the output of a previous *M(1)* (page 165)

> Let us consider a *M(1)* unit whose control variable is x^m [sic, x_m] and data inputs are *g* and *h*.
>
> > Without loss of generality, based on Shannon's expansion theorem, the logical output *f* can be expressed by
> >
> > $$f(g, x_i, X_m) = g\bar{x}_m + hx_m \qquad (1)$$
> >
> > Here *g* (called subfunction), is a function of binary variables (other than x_m), h can assume any one of the four values: 0, 1, x_i, or $\bar{x}_i$, where x_i is another variable other than x_m, x_m is either x_m or $\bar{x}_m$.

The symbol x_m refers to; the logical state, true or inverted, of the binary variable x_m (Tosser, page 64, § 2.1); for simplicity, we refer to x_m as x_m and $\bar{x}_m$ as $\bar{x}_m$. The logical output f of a 2:1 multiplexer is a function of three variables (g, x_i, x_m) where x_m is a binary variable at the control input (page 165); input *g* is a function of binary variables (other than x_m) and, so, is a binary variable; and *h* is a binary variable x_i (other than x_m) or a constant 0 or 1).

In the function "$g\bar{x}_m + hx_m$": the "+" (sum) term represents a logical "OR" operation; the product term "$g\bar{x}_m$" (also written as "$g.\bar{x}_m$") represents the logical "AND" of "g" and "$\bar{x}_m$ "; and the product term

"h x_m " (also written as "h.x_m") represents the logical AND of "h" and "x_m." That is, the function is ("g" AND "$\bar{x}_m$ ") OR ("h" and "x_m"). See Appendix B for a background description of logic expressions. The control variable x_m, is a control signal that causes the multiplexer to select the input "*h*" as the output when x_m =1, and causes the multiplexer to select the input "g" as the output when x_m =0 ($\bar{x}_m$ =1), as illustrated below.



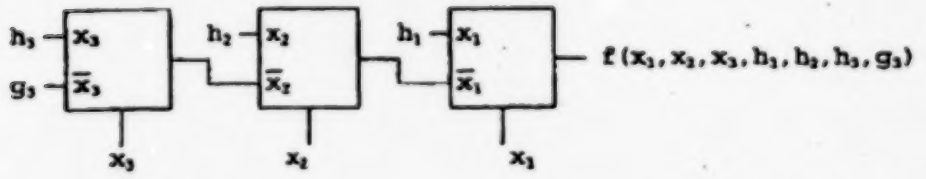
When x_m =1, the input *g* has no effect on the logic function and when x_m =0 ($\bar{x}_m$ =1), the input *h* has no effect on the logic function because these inputs are not selected.

The data inputs for an *M(1)* can be connected in two ways as shown in Figs. 2a and 2b, the only difference being that x_m and $\bar{x}_m$ are interchanged in the equations.

The rejection relies on Gorai's Fig. 3, which discloses a cascade (serial) arrangement of *p*-stages of 2-input multiplexers *M(1)*. A cascade (serial) network is one in which the output terminals of one network are directly connected to the input terminals of the other network. Each control input variable (x_1, . . ., x_{p-1}, x_p) is unique and controls only one M(1) . Each input variable "*h* can assume any

one of the four values: 0, 1, x_i, or $\bar{x}_i$, where x_i is another variable other than x_m " (page 165) . Each of the input variables (h_1, ..., h_{p-3}, h_p) can be unique, as evidenced from the previous discussion, or can be a constant or the same as a control input variable to implement a function of less than (2p+1) variables. Each of the subfunctions (g_1, . . . , g_{p-1} , g_p) "is a function of binary variables (other than x_m)" (page 165) (e.g., g_{p-1} is a function of the binary variables g_p, h_p and x_p from the previous stage) , where "[f] or the last stage, g_p is reduced to a single variable or constant 0 or 1" (page 166). Thus, for $p=3$, the network has three control input variables (x_1, x_2, x_3) and four data input variables (h_1, h_2, h_3, g_3), as recited in claim 47; and for p=4, the network has four control input variables (x_1, x_2, x_3, x_4) and five data input variables (h_1, h_2, h_3, h_4, g_4), as recited in claim 48.

The networks of 2:1 multiplexers in Gorai implement logic functions by appropriate selection of inputs using the control variables. For example, a general serial arrangement for p=3 in accordance with Fig. 3 is shown on the next page.



Using the multiplexer expressions in Gorai:

$$f = x_1h_1, + \bar{x}_1 (x_2h_2 + \bar{x}_2 (x_3h_3 + \bar{x}_3g_3))$$

$$= x_1h_1 + \bar{x}_1x_2h_2 + \bar{x}_1\bar{x}_2x_3h_3 + \bar{x}_1\bar{x}_2\bar{x}_3g_3$$

Thus, the multiplexer arrangement selects input h_1, when control variable x_1=1 (x_1 and x_1 are not part of the term x_1h_1, and so either can be 0 or 1) OR selects input h_2 when control variables $\bar{x}_1$=1 (x_1=0), x_2=1 , i.e., $\bar{x}_1x_2$=1 (x_3 is not part of the term $\bar{x}_1x_2h_2$ and so can be 0 or 1) OR selects input h_3 when control variables $\bar{x}_1$=1 (x_1=0), $\bar{x}_2$=1 (x_2=0) , x_3=1, i.e., $\bar{x}_1\bar{x}_2x_3$=1 OR selects input g_3 when control variables $\bar{x}_1$=1 (x_1=0), $\bar{x}_2$=1 (x_2=0), $\bar{x}_3$=1 (x_3=0), i.e., $\bar{x}_1\bar{x}_2\bar{x}_3$=1. The input selected for output is only a function of the control variables, which is, by definition, a multiplexer. See also Appendix C for a discussion of two examples in Gorai.

Tosser

Figures 6, 9, and 11 of Tosser each show a cascade of three 2-input multiplexers having 3 control inputs and 4 data inputs. it is this structure that is relied upon in the rejection. The figures show the data inputs connected to variables (including the control variables) and constants to realize specific functions of four variables. However, the multiplexer structure does not change depending upon the inputs, and the input variables are not part of the claimed structure.

Tosser discloses a graphical method for implementing logic functions using a cascade of 2^n-input multiplexers (abstract), and, in particular, using a cascade of 2-input multiplexers (page 65, left col.). The method is valid for any function that can

be represented on a Karnaugh map, i.e., with up to six variables (abstract). However, the rejection relies on the structure of a serial connection of three 2-input multiplexers, not on the method of implementing logic functions.

Weste

Weste discloses a 2:1 TGM circuit in Fig. 1.10 (page 17). "As the switches have to pass '0's and '1's equally well, complementary switches with n- and p-transistors are used. The truth table for the structure in Fig. 1.10 -is shown in Table 1.4." (Pages 14 & 16). When the input to a complementary switch is "1" the input ("0" or "1") is passed to the output, and when the input to the switch is "0," the input is not defined. There is no dispute that Weste teaches a transmission gate multiplexer (TGM) as claimed.

Weste discloses using TGMs to create logic circuits. (pages 172-175).[2]

Level of ordinary skill in the art

The level of ordinary skill in the art is evidenced by the references. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and

---

[2] It is apparent from the truth table and multiplexer connections that "XOR" (exclusive OR) in Table 5.1 (page 174) and Fig. 5.15 (page 175) should really be "Exclusive-NOR" (XNOR).

content of the prior art and the level of ordinary skill solely on the cold words of the literature"); In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (the Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record); Okajima v. Bourdeau, 261. F.3d 1350, 1355, 59 USPQ2d 1795, 1797 (Fed. Cir. 2001) ("[T]he absence of specific findings on the level of skill in the art does not give rise to reversible error 'where the prior art itself reflects an appropriate level and a need for testimony is not shown.'"). Skill in the art is presumed. See In re Sovish, 769 F.2d 738, 743, 226 USPQ 771, 774 (Fed. Cir. 1985).

Based on the references, we find that one of ordinary skill in the art would have a thorough understanding of digital logic circuits, in particular, the design of digital logic switching systems so as to be familiar with the terminology and concepts described in Gorai and Tosser, and would have sufficient skill to apply these teachings to specific problems. Such knowledge is commonly taught in an undergraduate computer science course on switching theory and logical design. One of ordinary skill in the art would also have knowledge of actual electrical implementations of multiplexers such as the transmission gate multiplexers taught in Weste. Such knowledge is commonly available in undergraduate courses in electrical engineering. circuits and electronics.

Differences

Between Gorai and the subject matter of claims 47 and 48

Gorai does not disclose the implementation of the 2:1 multiplexers and, so, does not disclose using TGMs.

Between Tosser and the subject matter of claims 47 and 48

Tosser does not disclose a cascade of four 2:1 multiplexers as recited in claim 48.

Tosser does not disclose the implementation of the 2:1 multiplexers and, so, does not disclose using TGMs.

The examples in Figs. 6, 9, and 11 of Tosser realize functions of only four variables. Nevertheless, the structure is capable of implementing functions of seven variables and it is the cascade multiplexer structure, not the application of the cascade multiplexer structure to realize a specific function, that is relied upon. The actual variables are not part of the claimed combination and, thus, the recitations of first, second, third, and fourth input variables are not differences: it is sufficient that the structure can accept four separate input variables and three separate control variables.

Objective evidence of nonobviousness

Objective evidence of nonobviousness (also called "secondary considerations") must always be considered in making an obviousness decision, Stratoflex v. Aeroauip, 713 F.2d at 1538, 218 USPQ at 879, although it need not be necessarily conclusive on the issue of obviousness, Ashland Oil. Inc. v. Delta Resins & Refrac., Inc., 776 F.2d 281, 306, 227 USPQ 657, 674 (Fed. Cir. 1985). A "nexus" is required between the merits of the claimed invention and the evidence of secondary considerations in order for the evidence to be given substantial weight in an obviousness decision. See Stratoflex, 713 F.2d at 1539, 218 USPQ at 879. "Nexus" is a legally and factually sufficient connection between the objective evidence and the claimed invention, such that the objective evidence should be considered in the determination of nonobviousness. See Demaco Corp. v. F. Von Langsdorff Licensing Ltd., 851 F.2d 1387, 1392, 7 USPQ2d 1222. 126 (Fed. Cir. 1988). The burden of showing nexus is on the applicant or the patent owner. See In re Huang, 100 F.3d 135, 139-140, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996) ("In the ex parte process of examining a patent application, however, the PTO lacks the means or resources to gather evidence which supports or refutes the applicant's assertion that the sales constitute commercial success.").

"It is well settled 'that objective evidence or [sic, of] non-obviousness must be commensurate in scope with the claims which the evidence is offered to support.'" In re Grasselli, 713 F.2d 731, 743, 218 USPQ 769, 778 (Fed. Cir. 1983) (citing In re Tiffin,

448 F.2d 791, 792, 171 USPQ 294, 294 (CCPA 1971)). The objective evidence is not commensurate in scope (coextensive) with the claimed subject matter if the claims are broader in scope than the scope of the objective evidence, e.g., if the product included elements or features not recited in the claims which may be responsible for the commercial success or praise. See Joy Technologies Inc. v. Manbeck, 751 F. Supp. 225, 229-30, 17 USPQ2d 1257, 1259-60 (D.D.C. 1990) (and cases cited therein), aff'd, 459 F.2d 226, 22 USPQ2d 1153 (Fed. Cir. 1992); Marconi Wireless Tel. Co. v. United States, 320 U.S. 1, 35 n.20 (1943) ("Marconi's specifications disclose a large number of details of construction, none of which is claimed as invention in this patent."); White v. Jeffrey Mining Machinery Co., 723 F.2d 1553, 1559, 220 USPQ 703, 706 (Fed. Cir. 1983) ("That Jeffrey's miner enjoyed commercial success does not support an implication that the jury found that a nexus existed between such success and the claimed invention, because the Jeffrey machine included several features not disclosed or claimed in the White patent.").

Inventor Tran's declaration

Patent owner argues that "[f]urther evidence of non-obviousness is set forth in a Statement Concerning Commercial Success and Other Objective Indicia of Non-Obviousness (attached as Exhibit H):" (Br22). Exhibit H refers to the Declaration Under 37 C.F.R. § 1.132 of the inventor Joseph Tran (Exhibit I to the brief) and states that "there is ample evidence of at least the commercial success that followed from this patent, as well as a suggestion of how it solved a

long-felt need" (Exhibit H, page 1). Exhibit H tracks Mr. Tran's declaration and we will discuss Mr. Tran's declaration in Exhibit I rather than the unsworn statements in Exhibit H. Neither Exhibit H nor Mr. Tran's declaration discusses "long-felt need."

The examiner's position is (EA22-23):

> [T]he final arguments concerning the alleged commercial success of the invention, as set forth in the Tran declaration under 37 CPR 1.132 (after reviewing this further evidence and looking at the issue of obviousness *ab initio*, taking all of the prior art, arguments, etc into account), the commercial success evidence/argument does not overcome the finding [sic, conclusion] of obviousness of the claims because the required nexus is not seen to exist, i.e., mere "potential licensing", the fact that other companies may have "lauded" the invention, etc, without more, is not seen to rise to the level of "commercial success', per se. Moreover, even if such a nexus did exist, this would not be sufficient to overcome the strong motivation to use the well-known TGM circuits of Weste to implement the "black box" multiplexers of both Gorai's Fig. 3 and Tosser's Fig. 9.

We agree with the examiner that no nexus has been established between the evidence and the claimed subject matter. Mr. Tran's declaration merely sets forth a number of documents without even trying to show that what is discussed is the

subject matter of claims 16 and 17 in the '666 patent (claims 47 and 48 in the reexaminations), much less trying to show a nexus. The only thing that might be considered "commercial success" is evidence of licensing to Intel Corp., which is usually treated as a separate category of objective evidence. There is no evidence of any sales of products containing the claimed subject matter that might be considered commercial success.

Mr. Tran states:

> 6. Accompanying this Declaration as Exhibit 1 is a copy of an article appearing in an on-line industry publication entitled *Silicon Strategies*, which is dated May 5, 1999, and is currently available at http://www.silicon strategies.com/sbn.news archive/1999/19990507a10.html. This copy is true and accurate as to the content of the publication as it first appeared.
>
> 7. The technology covered by the claims of the '666 patent is sometimes referred to as the "M-cell technology."
>
> 8. Accompanying this declaration as Exhibit 2 is a copy of an article in *The Portland Business Journal* dated May 6, 1999. Exhibit 2 is a copy of an on-line version of the article. This copy is true and accurate as to the content of the publication as it first appeared.

The declaration merely points to the articles and does not attempt to address how the articles

disclose what was actually licensed to Intel Corp. or how there is a nexus to the merits of claims 16 and 17 of the '666 patent. The article states:

> TransLogic Technology, Inc. here announced today that it has signed a five-year licensing agreement with Intel Corp., under which Intel will use TTI's computer-aided design (CAD) software tools and related technology to improve the performance of integrated circuits.

"Acquiescence by a substantial portion of the competitors in a market to the validity of a patent--generally through acceptance of a license--has been regarded as evidence supporting patentability. The theory behind use of commercial acquiescence is that persons would not usually act in a fashion contrary to their economic interests unless convinced of the patent's validity." 2 Donald S. Chisum, Patents § 5.05[3] (2003). What is said to be licensed is "computer-aided design (CAD) software tools and related technology." The '666 patent has nothing to do with CAD software tools. It is unknown what the "related technology" refers to, and we will not assume it includes or is limited to the '666 patent. Although evidence discussed infra, indicates that the '666 patent was part of the licensing deal, we only consider the article before us. A nexus requires evidence that the licensing was due to the merits of claims 16 and 17 of the '666 patent and not to other elements and services; i.e., the objective evidence must be commensurate in scope with the claims. This article does not show what was licensed, much less any nexus to the '666 claims. It would have been

easy for patent owner to provide a copy of the license agreement to show exactly what was actually licensed.

The article also states:

> TTI holds eight patents regarding IC technology. The company's patented M-cells are fully characterized transmission/pass gate programmable standard cells that help designers get the best performance from their IC designs. TTI also sells related software and a library of cells allowing customers to easily use its technology in design and development.
>
> The company's Tlogic software enables M-cells to be utilized during the logic synthesis process. By integrating Tlogic with the leading synthesis tools, IC designers will have all the benefits provided by the M-cells without having to change their current design methodology.

As written, this seems to be a description of TTI's products and company goals rather than what was actually licensed. In any case, Tlogic software has nothing to do with '666 patent, which is directed to multiplexer hardware, nor is there any evidence that "integrating Tlogic with the leading synthesis tools" was an object of the Intel licensing (this appears to refer to talks with Cadence Design Systems, Tran declaration ¶¶ 10-13).

Mr. Tran states that "[t]he technology covered by the claims of the '666 patent is sometimes referred to as the 'M-cell technology'" (¶ 7). There is

no indication in the article that what was licensed was M-cell technology. Moreover, there is no evidence that "M-cell technology" is limited to claims 16 and 17 of the '666 patent. As discussed infra, there are statements that "M cell" was used by Intel to refer to the subject matter of two other TTI multiplexer patents in addition to the '666 patent. The term "cell" in "M-cell" also suggests something more than the bare multiplexer circuit. A "cell" is a small scale logic circuit for which the layout of a mask pattern for integrated circuit fabrication has already been finished (Yano et al., U.S. Patent 5,581,202, col. 1, lines 19-21, Figs. 1A & 1B, Exhibit 9 to Tran declaration). This raises the question of whether "M-cell" includes a layout pattern and mask implementation in addition to the multiplexer circuit itself. Mr. Tran's statement that "[t]he technology covered by the claims of the '666 patent is sometimes referred to as the 'M-cell technology'" (¶ 7) implies that the '666 patent claims are commensurate in scope with M-cell technology, but this has not been shown to be true and conflicts with statements that "M-cell technology" includes other patents. If M-cell technology includes additional components (design software, actual cell layouts, other kinds of multiplexer circuits, other patents, etc.) that are not part of the '666 multiplexer claims, there is no nexus between M-cell technology and the merits of the '666 patent. We will not speculate that M-cell technology is commensurate in scope with the claims of the '666 patent or that it is what was licensed.

Exhibit 2 is a shortened version of Exhibit 1 and adds no new information.

The evidence of licensing to Intel is not entitled to any weight because it has not been established what was licensed or shown that there is a nexus between the licensing and the merits of claims 16 and 17 of the '666 patent. Mr. Tran's belief that the '666 patent was the reason for the license is not evidence.

Mr. Tran next states:

> 9. Before 1999, several key players in the integrated circuit market were introduced to TTI's M-cell technology and came to appreciate its advantages over other conventional designs.

This is merely an introductory paragraph to the next set of Exhibits. Again, it is not known what is encompassed by the term "M-cell technology."

Mr. Tran's declaration continues:

> 10. One of these players, Cadence Design Systems, is today "the world's largest supplier of electronic design technologies, methodology services, and design services" (as appearing at http://www.cadence.com/company/index.html, on September 16, 2003, copy attached as Exhibit 3). Cadence sells design synthesis tools that allow the use of TTI's Tlogic software to enable designers to use M-cells in their designs.

The first sentence is not questioned. The second sentence merely says that Cadence's design synthesis tools allow the use of TTI's Tlogic software,

not that the Tlogic software was ever actually part of Cadence's design synthesis tools. The '666 patent is directed to a multiplexer structure, not design synthesis software and not the cell design.

The discussion of Cadence continues:

> 11. Cadence met with TTI to review the M-cell technology in 1993, a few months after the '666 patent was issued in December, 1992. In Cadence's internal report of the meeting, the new M-cell technology was lauded as "simple and elegant," "appealing," and offering advantages over conventional approaches:
>
> > The presentation from Translogic showed us a simple and elegant way to construct multi-level logic using CMOS inverters and N Channel transmission gates. The primary use of this technology would be the construction of a new type of cell called M cells that could replace conventional logic gates in logic synthesis and P&R. The technology is appealing in that a small number of M cells (e.g. a library of only a dozen cells) could replace a much larger library of

> conventional logic gates while offering smaller area and lower path delay realizations.

> 12. A copy of the internal Report from Jake Buurma to Jim Solomon, which is entitled "Debriefing from initial Translogic Meeting" and is dated March 26, 1993, is attached as Exhibit 4.

> 13. Cadence's report noted some areas where more information and development were needed, which is to be expected with developing technology, but concluded that "[i]f M cells prove effective for a wide range of logic functions and our tools can be adopted to efficiently use M cells, then we should consider adding a small library of M cells" to some of its products sold for integrated circuit design. Exhibit 4 at page 3.

There is no disclosure that the "M cells" being discussed correspond to the multiplexer structure of the '666 patent and, hence, there is no nexus. Even if it assumed that "M" stands for "multiplexer," patent owner owns U.S. Patent 5,040,139 ('139 patent), issued August 13, 1991, entitled "Transmission Gate Multiplexer (TGM) Logic Circuits and Multiplier Architectures," so there is no certainty that the discussion was limited to the '666 patent series multiplexer. The reference to "cells" implies a mask pattern layout for integrated circuit implementation, and what may have been advantageous was the cell implementation rather

than the multiplexer circuit itself. In any case, the internal report simply represents impressions from a meeting and does not constitute licensing, a commitment to license, or anything that could be considered a recognized category of evidence of nonobviousness. At best, the report indicates that there was interest in "M cells" (whatever they are). Certainly, there is no evidence of sales that would constitute commercial success. The Cadence evidence is not entitled to any weight.

The declaration continues:

> 14. TTI also met with National Semiconductor in 1993. Following this meeting, an August 7, 1993 letter was sent by Thomas L. Humphrey, Director of Business Development of National Semiconductor, to Mr. Joseph Tran. A true and accurate copy of the August 17, 1993 letter is attached as Exhibit 5.
>
> 15. As expressed in Exhibit 5, National recognized TTI's then-ongoing efforts in working with Cadence to develop design synthesis software for implementing M-cells and to test the software, expressing strong interest:
>
> > We at National Semiconductor are definitely interested in becoming such a Beta Site. As you know National works closely with Cadence. Availability of

> your design methodology on Cadence tools would be a major factor in making it accessible to the National design community ....
>
> 16. As also expressed in Exhibit 5, National Semiconductor recognized TTI's proprietary rights in its innovations, noting that "should our evaluation be positive and associated costs and licensing fees be justified," National would consider adopting the technology.

The letter refers to a "proposal to Cadence to jointly develop a design automation software package that implements Translogic's design methodology" and "[a]vailability of your design methodology on Cadence tools would be a major factor in making it accessible to the National design community." Thus, the letter concerns a "design methodology," not a multiplexer hardware circuit as in the '666 patent. Moreover, the letter does not say anything about the merits of the unidentified methodology: it only states that the methodology might be adopted "should our evaluation be positive," indicating that it had not been evaluated. The letter expresses polite interest in the technology and in becoming a Beta test site if Cadence agrees to adopt TTI's design methodology. The "technology" is not identified as the series multiplexers of the '666 patent and it could be TTI's "design methodology." The letter does not constitute licensing, a commitment to license, or anything that could be considered a recognized category of evidence of

nonobviousness. Certainly, there is no evidence of sales that would constitute commercial success. The National Semiconductor evidence is not entitled to any weight.

Mr. Trans [sic] states:

> 17. TTI had also presented its M-cell technology to Hewlett Packard (HP). Following a meeting with HP, TTI received an August 3, 1993 letter from Eric Larson, ICBD Marketing Manager and Acting General Manager. A true and accurate copy of this letter is attached as Exhibit 6.
>
> 18. As indicated in Exhibit 6, HP declined an offer to work on a joint development project with TTI, but as in the case of National Semiconductor, expressed interest if design synthesis software to implement TTI's M cell technology became available:
>
> > I am encouraged to hear, however, of the negotiations with a major CAD software supplier. As we discussed, a relationship resulting in a market ready software implementing the TransLogic Design from the major CAD supplier would be a major step forward. As I understand from your business model,

> users would purchase software from the major CAD supplier and would obtain a license from TransLogic Design for the application of the technology in the user's products. Assuming the software cost is consistent with similar packages and the technology fee is appropriate in relation to the added value of the design improvements, the model you described could be of interest for many applications we see in ICBD.

The letter states (Exhibit 6):

> As you know, we have investigated the TransLogic Design methods and have considered the possibility of joint development of the software for our applications. We continue to be interested in the technology, however because of previous resource commitments and priorities, we are unable to work on joint development.

The subject of the letter is design "methods" and "software," whereas the '666 patent deals with multiplexer hardware, so there is no apparent nexus to the subject matter of the '666 patent claims. The letter indicates polite interest in the technology, but

no identification of the technology or indication that the technology had been evaluated. The letter does not constitute licensing, a commitment to license (it states that "it is premature to make a commitment"), or anything that could be considered a recognized category of evidence of nonobviousness. There are no sales that would constitute commercial success. The Hewlett-Packard letter is not entitled to any weight in the obviousness determination.

Mr. Tran states:

> 19. Earlier, HP had requested me to synthesizee two conventional HP circuits using M-cells in place of at least some typical logic gates. The M-cell modified circuits were then compared to the corresponding conventional logic gate circuits. The results were reported in an October 16, 1991 letter from Don Morris to Stan Dallas. A true and accurate copy of this letter is attached as Exhibit 7.
>
> 20. The results reported in Exhibit 7 demonstrate the advantages of the M-cell technology. The M-cell modified circuits were found to be "22%r to 33% faster and 2% to 24% more dense" than the corresponding conventional logic gate circuits. Indeed, HP commented that "HP feels that these results prove that the technology has merit."
>
> 21. Stan Dallas sought confirmation of the test results in an October 23, 1991 letter to Don Morris, and Don Morris confirmed the results in his reply. A true and accurate copy

of this letter with Don Morris' handwritten reply is attached as Exhibit 8.

The letter discusses that two test circuits selected by HP, and synthesized by Mr. Tran, had better performance and higher density than standard cell designs. The test circuits and how the test circuits were implemented are not described in the letter; the letter mentions a "basic logic cell," but does not identify it as a serial multiplexer circuit as claimed in claims 16 and 17 of the '666 patent (now claims 57 and 48). As of the date on the letter, October 16, 1991, Mr. Tran had the '139 patent, issued August 13, 1991, to TGM logic circuits and multiplexer architectures, and the application which matured into the '666 patent had been filed March 15, 1991, but not yet issued, so the letter might equally well refer to the '139 patent. The letter does not use the term "M-cell," but even if "M-cells" referred to the multiplexer of the '666 patent, it can be referring to the 2-stage serial multiplexer of Fig. 2, whereas the claims are directed to 3-stage and 4-stage multiplexers. Only original '666 patent claims 16, 17, 25, and 26 were limited to more than two stages, and the claims have been limited in this reexamination to 3-stage and 4-stage multiplexers because prior art disclosed the 2-stage multiplexer; see, e.g., Fig. 2 of Japanese Laid Open Patent Application H1[1989]-256219 to Goto (Goto '219 application). No nexus has been established between the contents of the letter and the 3-stage or 4-stage multiplexer subject matter of the '666 patent. The letter does not constitute licensing, a commitment to license, or anything that could be considered a recognized category of evidence of nonobviousness.

There are no sales that might constitute commercial success. The Hewlett-Packard letter is not entitled to any weight in the obviousness analysis.

22. As further objective indicia of nonobviousness, I point out that approximately two years after the '666 patent was granted to TTI, Hitachi filed a patent application in November 1994 that issued as U.S. Patent No. 5,581,202 (hereafter the '202 patent) to Dr. Kazuo Yano and Yasuhiku Sasaki. (Hitachi is the requesting party in this and each of the previous reexamination proceedings.) The '202 patent describes a circuit using two 2:1 multiplexers connected in series. Figure 8(b) of the patent shows 4:1 and 5:1 serial multiplexers similar to the 4:1 and 5:1 serial TGM multiplexers described in the '666 patent. During prosecution of the application that matured into the '202 patent, Hitachi represented to the U.S. Patent and Trademark Office that the circuits shown therein were patentable and not obvious. A true copy of the '202 patent is attached as Exhibit 9.

23. The subject matter of the '202 patent was further described in an article co-written by the Dr. Yano called "Lean Integration: Achieving a Quantum Leap in Performance and Cost of Logic LSIs," IEEE 1994 Custom Integrated Circuits Conference, 1994. A true copy of this article is attached as Exhibit 10.

It is not explained what category of objective evidence this evidence is supposed to fit in or how it tends to show nonobviousness of patentee's invention. The Yano '202 patent and the Yano paper do not assert that they invented the serial multiplexer. The 1994 Yano paper discloses a 2-stage TGM (the Y_1 logic cell in Fig. 1), but does not disclose a 3-stage or 4-stage TGM. Since the '666 patent discloses a 2-stage TGM (Fig. 2), and since only claims 16, 17, 25, and 26 of the '666 patent are limited to more than two stages, it appears that patent owner considered the Yano paper to disclose the '666 invention. However, the claims have been limited in this reexamination to 3-stage and 4-stage multiplexers because prior art disclosed the 2-stage multiplexer; see, e.g., Fig. 2 of Goto '219 application. Thus, the Yano paper is not evidence of nonobviousness.

Mr. Tran's assertion that "[d]uring prosecution of the application that matured into the '202 patent, Hitachi represented to the U.S. Patent and Trademark Office that the circuits shown therein were patentable and not obvious" (¶ 22) is not supported by evidence from the prosecution history showing that it was represented that the circuits of Fig. 8B were patentable. Applicants do not assert that everything in the specification and drawings is novel and nonobvious: applicants only assert that the claimed invention is patentable over prior art known to them. The claims of the '202 patent are not directed to the '666 multiplexer circuits. There is no evidence of copying. The Yano '202 patent and the Yano paper are not entitled to any weight in the obviousness analysis.

Supplemental court documents

On May 19, 2005, patent owner filed an Information Disclosure Statement (IDS) under 37 C.F.R. §§ 1.555 and 1.98 providing a copy of numerous court documents from Translogic v. Hitachi, including: (1) transcripts from jury trial on damages (Vols. 1A, 1B, 2A, 2B, 3A, 3B, and 4A); (2) order of February 22, 2005, granting plaintiff's motion for summary judgment of infringement; (3) Hitachi's Emergency Motion for Stay of Permanent Injunction dated May 12, 2005; (3) district court order granting permanent injunction entered May 12, 2005; (4) verdict form (finding inducement of infringement and awarding $86.5 million in damages for infringement); (5) transcript of verdict proceedings of May 6, 2.005; (6) Welcome to the family - the SuperH RISC Engine Family of 32-bit RISC Microcomputers, HITACHI Today, Vol. 38 (Winter 1997); (7) HITACHI Technology PARTNER, Design Solutions from Hitachi Semiconductor (America) Inc. (July/August 1998); and (8) Civil Docket for Case #: 3:99-cv-00407-PA, Translogic Technology, Inc. v. Hitachi, Ltd. et al., U.S. District Court, District of Oregon (Portland). Patent owner asserted that "[c]ertain of these documents pertain directly to objective indicia of non-obviousness including commercial success, licensing, and copying of the invention as claimed in the pending merged reexaminations," referring to licensing by Intel Corp. and the commercial success and widespread use of products incorporating the claimed invention.

At the oral hearing on May 31, 2005, this panel gave the patent owner one week to file a paper

describing how the various documents evidenced nonobviousness. We indicated that the panel would exercise our discretion in deciding whether to consider this new evidence. Patent owner timely filed a statement on June 6, 2005 (pages referred to as "S__").

The purpose of an IDS in a reexamination proceeding is to satisfy the duty of the individuals associated with the patent owner to disclose to the Office all information known to be material to patentability. See 37 C.F.R. § 1.555(a). That is, an IDS presents evidence which bears on the issue of unpatentability, not patentability. Because all of the claims stand rejected, there is no reason to remand the case to the examiner for consideration of the IDS. The reexamination proceedings have already gone on long enough. Although we are not required to consider patent owner's statement, we nonetheless do so because a patent is involved. We address only the arguments actually presented by patent owner. Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."). Patent owner is precluded from raising new arguments on appeal. See In re Watts, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("Just as it is important that the PTO in general be barred from raising new arguments on appeal to justify or support a decision of the Board, it is important that the applicant challenging a decision not be permitted to raise arguments on appeal that

were not presented to the Board." (Footnote omitted.)).

Patent owner states in the introductory paragraph (51-2):

> These itemized portions pertain to objective indicia such as licensing, initial skepticism and praise, commercial success, and copying of the claimed invention. As used herein, any products designated as "infringing" were found to infringe original claims 16 and 17 that remain pending (but are renumbered) in the merged reexaminations. The portions designated below in combination with other materials such as, for example, Mr. Tran's Declaration Concerning Commercial Success, establish that the invention of claims 16 and 17 provides results that are surprising to those of skill in the art, was praised by those of skill in the art by, for example being licensed for use in the Pentium 4 processor, and has demonstrated commercial success in a variety of products.

The items are listed in the statement with no explanation of how they fit into a category of evidence of nonobviousness or how there is a nexus to the merits of the claimed invention, e.g., "Statement by Mr. Axelrod [attorney for Hitachi] that all Hitachi SH-4 products include infringing circuit segments (at 46)" (S2) and "Testimony by Mr. Tran concerning software needed for automated inclusion of patented multiplexer circuits (at 8)" (S2). Patent owner essentially leaves it to us to do the

analysis for it. For this reason alone, the statement is unpersuasive. Nevertheless, we have tried to determine how the various statements might be considered to be evidence of nonobviousness.

Although patent owner refers to "initial skepticism" we find no statements which might fall into this category. Although patent owner refers to "copying of the claimed invention," none of the statements deals with "copying." It was asserted by defendants in the district court that there was no evidence of copying because the creation of circuits that give rise to claims in dispute were almost always by EDA (Electronic Design Automation) synthesis software (opening statement by Mr. Axelrod, attorney for defendant Hitachi, Vol. 1A, p. 55, lines 13-22; testimony of Mr. Hattori, Vol. 2B, p. 110, line 21, to p. 111, line 9). As far as we can determine, there is no evidence of copying. In any case, "more than the mere fact of copying by an accused infringer is needed to make that action significant to a determination of the obviousness issue." Cable Electric Products, Inc. v. Genmark, Inc., 770 F.2d 1015, 1028, 226 USPQ 881, 889 (Fed. Cir. 1985). "[Copying] may have occurred out of contempt for the specific patent in question." Id. There is no doubt in this case that Hitachi considered the '666 patent to be invalid.

The statements break down into four categories:

(1) commercial success of defendant Hitachi's processors; (2) licensing to Intel; (3) performance of the '666 circuits and statements about Dr. Yano's

paper and '202 patent; and (4) statements by Intel about TTI technology.

(1)

The "commercial success of products incorporating the claimed invention" (S5) relied upon by patent owner is the commercial success of Hitachi's SH-3 and SH-4 series microprocessors, which includes circuit segments which were found to infringe '666 patent claims 16 and 17 (rewritten here as claims 47 and 48) and which are incorporated in products by SnapGear, Compaq, Medtronic, Sega of America, Casio, Inc., LexMark, and others (S2-4). The argued commercial success is not due to any product by the patent owner. It is stated that "Intel licensed the patented technology for use in one of the most important products ever introduced, the Pentium 4" (S2). However, TTI's technology was never used in the Pentium 4 and the Pentium 4's success does not count as commercial success. It is stated that $62 million is the approximate total value of U.S. sales of infringing Hitachi products (S3). References to infringement, use of patented technology, and the amount of Hitachi sales of infringing products fall into this category.

Commercial success of an infringer's success and success of others may be entitled to weight. See 2 Patents § 5.05 [2] [g] . However, patent owner has not even attempted to establish a nexus between the commercial success of Hitachi's microprocessors and the merits of the claimed invention. The SH3 and SH-4 series microprocessors are complex, high-performance RISC (reduced instruction set

computer) microprocessors verified to be compatible with the Windows CE operating system and designed to offer low power consumption and to be used with a wide range of multimedia and communication products; see HITACHI Technology PARTNER under News Briefs and HITACHI Today. Testimony indicates that the infringing circuit segments formed an extremely small fraction of the overall microprocessors. For example, the percentage of transistors in the infringing circuits in the 7705 SH-3 (SH7705) microprocessor of the 5.2 million total number of transistors was 0.0064 percent (Vol. 2B, p. 112, lines 1-14) and the percentages of transistors in the infringing circuits to the total number of transistors in the 7750 SH-4 (SH7750) and 7760 SH-4 (SH7760) processors were 0.0056 percent and 0.0019 percent, respectively (Vol. 2B, p. 112, line 15, to p. 113, line 6). There were about 184 transistors in the infringing circuits and the SH7750 has about 3.3 million transistors and the SH7760 has almost 10 million transistors (opening statement of Mr. Axelrod, Vol. 1A, p. 46, line 22, to p. 47, line 3). There is no showing whatsoever that the success of the Hitachi microprocessors, and the products that they were part of, were due, even in part, to the merits of the '666 patent. In addition to failing to show that the commercial success was not due to unclaimed features of the operation of the 99.99% of the transistors in the microprocessors, patent owner has failed to address all the usual reasons why commercial success may not demonstrate a nexus to the merits of the claimed invention, such as advertising, seller's dominant market position, etc. Accordingly, no nexus has been established. The evidence of commercial success of Hitachi's

microprocessors and of the products that they were part of is not entitled to any weight in the obviousness determination.

(2)

The terms of the Intel license from TTI are not complete. The total value of the deal was $5 million and involved TTI patents, 5,040,139, 5,162,666, and 5,200,907 (testimony by Mr. Tran, Vol. 1B, p. 53, line 2, to p. 54, line 12). The deal was for $5 million over five years (testimony by Mr. Tran, Vol. 1B, p. 59, line 20). Intel internally assigned a value of $3.5 million to the three patents (testimony by Mr. Napper, witness for defendant, Vol. 3B, p. 6, lines 16-19). As stated in the opening statement by Mr. Axelrod, Vol. lA, p. 61, line 9, to p. 62, line 17):

> What Intel negotiated for and got were 25 licenses to the software that Translogic developed. That includes the library products that you'll hear testimony about. This software and this library is basically the work product or end result of what it was that Translogic had been developing with many, many dollars of investors' money over a number of years.
>
> Then they got support, maintenance and upgrades to that software capability from Intel for over a period of five years. Mr. Tran will testify about what that support involved. He has testified previously sometimes it involved his entire company coming to work - not coming to work but supporting Intel or working on a particular problem Intel may

have. So it was not an insignificant commitment.

Then you will see in the course of their negotiations Intel insisted that it get license rights to all three of the patents, very different patents, that use this transmission gate technology that Intel was interested in and thought it might use in connection with the Pentium 4 product that was going to be coming out.

So it got rights to all three patents. I think they refer to them in the Intel license as the M cell patents. Then it got a release of any of the claims that Translogic may have had that Intel had done something in the past that infringed. You have this bundle as one reference point, and you kind of have to sort out through that.

The parties will give you very conflicting views. I think Mr. Love indicated they will want to say: Well that was all given to them for free, and the only thing that counted was the '666 patent, and we even discounted that. That's one of the things that you will be asked to evaluate.

See also Testimony of Mr. Scanlon (Vol. 2A, p. 94, line 17, to p. 96, line 21); closing arguments of Mr. Elkins, Vol. 3B, p. 115, lin 18, to p. 117, line 19). Thus, the license apparently included many components in addition to the multiplexer circuit of the '666 patent. Although Mr. Tran testifies that it is his opinion that the main value is in the '666

patent (Vol. 1B, p. 54, line 18, to p. 56, line 4), we find no evidence that Intel considered the '666 patent to be the main reason for the license. Patent owner could have, but did not provide a copy of the license agreement so that it could be evaluated. The license agreement could clarify the meaning of the term "M cell," which Mr. Tran uses to refer to the '666 patent, but which was apparently used by Intel to refer to all three patents. No nexus has been established between the Intel licensing agreement and the merits of the '666 patent and the licensing agreement is not entitled to any weight.

Moreover, Intel took a license after TTI had discussions with Hitachi and was considering suing Hitachi for infringement. Intel apparently considered licensing TTI's patents to avoid litigation costs. See Question by Mr. Elkins, attorney for defendants, on cross-examination (Vol. 2A, p. 100, lines 17-20: "[P]age 5 of Exhibit 266 . . . indicates that Intel apparently saw the benefit to taking a license because it would mitigate patent infringement risks." "[Licensing programs] are not infallible guides to patentability. They sometimes succeed because they are mutually beneficial to the licensed group or because of business judgments that it is cheaper to take licenses than to defend infringement suits, or for other reasons unrelated to the unobviousness of the licensed subject matter." EWP Corp. v. Reliance Universal Inc., 755 F.2d 898, 907-908, 225 USPQ 20, 26 (Fed. Cir. 1985). Intel could have decided that it was cheaper to take a license to all of TTI's patents than to get involved in an infringement suit. Thus, no nexus has been established between the Intel license agreement and

the merits of the '666 patent, and the license agreement is not entitled to any weight in the obviousness determination.

(3)

Several items deal with test results from tests run by Intel and Hewlett-Packard (testimony by Mr. Tran, Vol. IA, pp. 81-83; Vol. 1B, pp. 3-9). Patent owner has not provided any copies of the test results and there is no way of telling what was tested or what it was compared against or what the results were. The testimony of Mr. Tran is not clear as to exactly what was tested or what was superior in the test results. Some of the testimony indicates that the results were dependent on Mr. Tran's implementation of the multiplexer; e.g., "I need to design it, to lay it out, to extract it, to characterize test it -- after that, the real testing data that it produced, to see that the result of the testing, how fast the multiplexer would be in the real condition of the process that Intel have at that time" (testimony by Mr, Tran, Vol. 1A, p. 82, lines 5-10). We will not speculate on what was actually tested or what the test results show; the tests might just show measured results with no conclusion of whether the results are ordinary or unexpectedly good. Patent owner could have provided actual copies of the tests. The testimony of Mr. Tran referred to in the statement concerning the testing by Intel and Hewlett-Packard does not prove a nexus to the claimed invention and is not entitled to any weight

The statement also refers to "Testimony by Mr. Tran concerning promotion of serial multiplexer

technology, referred to as Y-cell technology, in Hitachi premier product (SH-4), praise for remarkable speed improvement obtainable with serial multiplexer technology as noted by Mr. Yano's '202 patent, and statement that increased speed is available with a power reduction of 23% ([Vol. 1B] at 10-18)" (S2). These statements appear to be just Mr. Tran's personal interpretation of the facts. While the SH-4 series microprocessors were found to contain 4:1 and 5:1 serial multiplexers under the '666 patent, there is no evidence that Hitachi "promoted" serial multiplexer technology or that it even knew that it contained this circuitry. It is true that the Yano '202 patent shows 4:1 and 5:1 serial multiplexers in Fig. 8B, but this is not Yano's claimed invention; the figure shows many ways to arrange multiplexer circuits, none of which was claimed. Mr. Tran's testimony does not demonstrate a nexus between the Yano patent and article and the merits of the claims 16 and 17 of the '666 patent and is not entitled to any weight in the obviousness determination.

(4)

The statement refers to statements by Mr. Love, one of TTI's attorneys, referencing an Intel document that states: "Reduces interconnects and improves performance of RLS. Provides faster, denser, lower-power synthesized logic. Is target for deployment in Northwood." (Vol. 3B, p. 103, lines 13-15.) We do not have a copy of this document and do not know the context of the statement. Perhaps the statement refers to all three TTI patents, which deal with multiplexers. These statements, in isolation, provide no nexus to the merits of the '666 patent.

The statement also refers to a "Statement by Mr. Love referencing an Intel statement concerning lack of alternatives to patented technology ('There's no substitute at this time.') ([Vol. 3B] at 107)" (S4) The full quotation is "Don't use TTI technology. There's no substitute at this time." (Vol. 3B, p. 107, lines 7-8.) It is ambiguous whether this means there are no alternatives to TTI's technology or that Intel was not planning to substitute TTI's technology in their product. We do not have a copy of this document and we do not know the context of the statement. This Intel statement, in isolation, provides no nexus to the merits of the '666 patent. Accordingly, the statements of Mr. Love are not entitled to weight in the obviousness determination.

Conclusion regarding objective evidence

For the reasons discussed above, we find that no nexus has been established between the evidence and the merits of claims 16 and 17 of the '666 patent (now claims 47 and 48). The evidence is not entitled to any weight in the obviousness determination.

Motivation

Whether there is motivation to combine the references is a question of fact drawing on the factors of Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966.) See McGinley v. Franklin Sports, Inc., 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001). This is a fifth factual finding.

The networks in Gorai and Tosser are only block diagrams and must be implemented with

actual, physical circuits to be useful. One of ordinary skill in the art would have recognized that any known 2:1 multiplexer circuit could be used to implement the 2:1 multiplexers in Gorai and Tosser. Weste teaches that 2:1 TGM circuits were well known in the logic design art. The motivation to combine flows from the fact that physical circuits are needed to implement the multiplexer blocks in Gorai and Tosser, and because TGM circuits were a well-known multiplexer implementation to those of ordinary skill in the art as taught by Weste.

Obviousness conclusion

One of ordinary skill in the art at the time of the invention would have been motivated to use 2:1 transmission gate multiplexers (TGMs) as taught by Weste for the 2:1 multiplexers in the series arrangements of multiplexers in Gorai and Tosser because one skilled in the art would appreciated that any conventional multiplexer circuit could be utilized to implement the 2:1 multiplexer blocks in Gorai and Tosser, and because TGMs were well-known multiplexer circuits as evidenced by Weste. We determined that the objective evidence of nonobviousness is not entitled to any weight in the obviousness determination because no nexus has been shown to the merits of the subject matter of claims 16 and 17 of the '666 patent (claims 47 and 48 in these reexaminations). Nevertheless, even if the evidence was somehow related to the merits of the '666 patent, it would not overcome the very strong case of obviousness. The evidence does not show that TGMs would have been a nonobvious multiplexer implementation.

Arguments

Patent owner's arguments were considered in making the obviousness determination, but were not convincing for the following reasons.

(1)

Patent owner argues that a *p*-stage Gorai circuit can receive only (*p*+1) variables (*p* control variables plus 1 input variable) and, therefore, the 7 input terminals of a 3-stage Gorai circuit is configured to realize a function of only 4 different variables instead of 7 variables as claimed (Br14-15; RBr6-8). It is argued that in the general *p*-stage multiplexer network arrangement of Fig. 3, the control inputs (x_1, ..., x_{p-1}, x_p) and g_p input are variables, but the h_k inputs must be a constant (0 or 1) or one of the variables (x_1, ..., x_{p-1}, x_p, g_p) (Br15).

This argument is based on the statement in Gorai that "an *M*(*p*) can realise any function of (*p*+1) variables" (page 164) and is incorrect for several reasons. First, the statement means that all possible functions of (*p*+1) variables can be realized, not that only functions of (*p*+1) variables can be realized; see Appendix A for a technical explanation. Second, Gorai discloses that "an *M*(*p*) having $p + k$ ($= p + 2^p$) inputs has the potential of realising functions of up to ($p + 2^p$) variables" (page 164), so an M(p) is clearly not limited to functions of (*p*+l) variables. A 2:1 multiplexer (p=1, 2^p=2) can realize functions of up to three variables: one control variable and two input variables. Third, Gorai discloses that for each stage the data input "*h* can assume any one of the four

values: 0, 1, x_i or $\bar{x}_1$ where x_i is another variable other than x_m [the control variable for that stage]" (page 165). The input variable x_1 is not required to be, but can be, a function of one of the control variables x_m. Fourth, the statement about $M(p)$ does not apply to a cascade of 2:1 multiplexers: an $M(p)$ is a conventional multiplexer with p control lines to select one of $k=2^p$ inputs to output on the output line. Because each input to a multiplexer can be a different variable, the cascade circuit in Fig. 3 can accept $(2p+1)$ different variables (p control variables and $(p+1)$ input variables); thus, a 3-stage network would have three control variables and four input variables as recited in claim 47, and a 4-stage network would have four control variables and five input variables as recited in claim 48.

(2)

It is argued that the examples in Gorai and Tosser lack the requisite number of input terminals for control and input variables to perform a multiplexing function.

Gorai

It is argued that the combinational circuits in the examples in Figs. 6, 8, 9, and 10 of Gorai "all fail to show or include three cascaded 2:1 multiplexers coupled to receive seven variables (four input variables and three control signals) or nine variables (five input variables and four control signals) as recited in the pending claims" (RBr7).

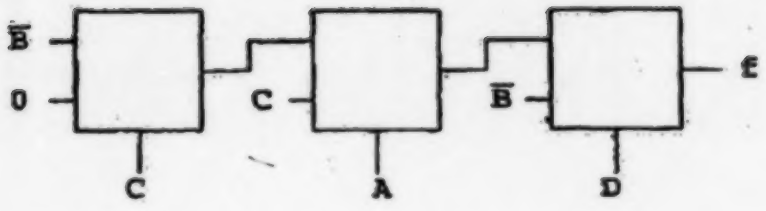
To keep the analysis simple, the rejection over Gorai relies on the general p-stage cascade

multiplexer circuit taught in Gorai's Fig. 3 and the corresponding text. This cascade multiplexer arrangement has inputs for p control variables and $(p+1)$ input variables. Thus, a 3-stage multiplexer has inputs for three control variables and four different input variables, as recited in claim 47, and a 4-stage multiplexer has inputs for four control variables and five different input variables, as recited in claim 48. The fact that the examples apply this multiplexer structure to realize functions of only four variables does not change the multiplexer structure.

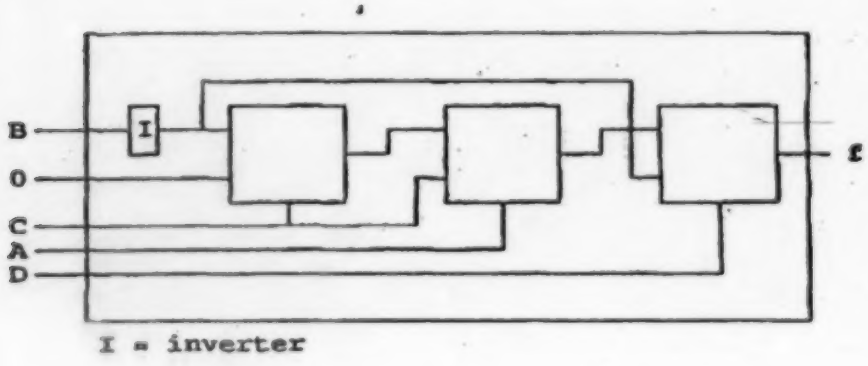
Tosser

It is argued that the circuit in Fig. 9 of Tosser, relied upon by the examiner, is only coupled to receive two different input variables, D (or $\overline{D}$) and C, where "0" is a constant (Br12-13), and "a circuit coupled to receive only two input variables cannot be a 4:1 multiplexer that must necessarily be coupled to receive four different input variables in order to select one of the four different input variables as an output" (Br13). It is argued that Fig. 9 discloses coupling the same variable (C or $\overline{C}$) to both a control input terminal and a signal input terminal and, "[b]ecause Tosser's, Fig. 9 circuit does not distinguish input variables and control signals, Tosser's Fig. 9 circuit cannot perform a 4:1 multiplexing function" (Br16).

Patent owner also argues that Tosser's Fig. 6 does not show a 4:1 serial multiplexer. Figure 6 of Tosser is shown below.



Patent owner presents the following figure adapted from Tosser's Fig. 6:



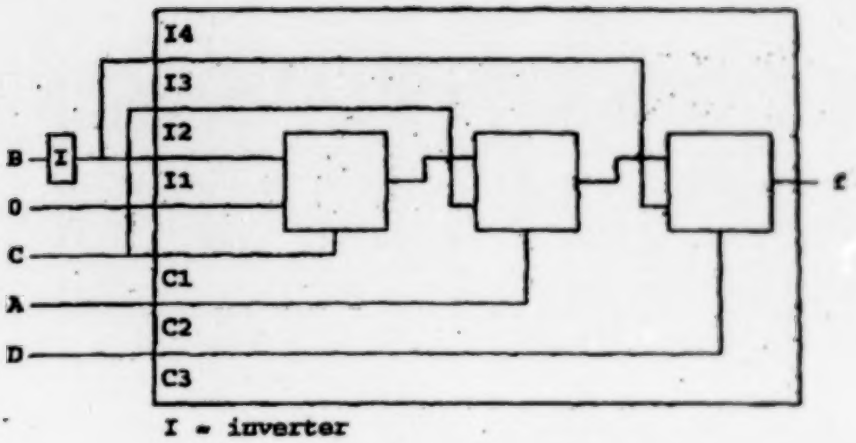
It is argued (Br16):

> This circuit is configured to receive at most four input variables (*A,B,C,D*). One input (*C*) is coupled to a control input of the first stage and to a signal input of the second stage. Thus, this three stage cascade also lacks any distinction of control signals and input variables as recited in the subject claims. In addition, only two inputs (*B,C*) are coupled to

signal input terminals, and only these two inputs can be coupled to the output. Inputs (*A,D*) are coupled only to control inputs and cannot be selected for coupling to the output. Thus, this circuit cannot perform the multiplexing function of the claimed 4:1 serial multiplexer circuits.

It is argued that expert opinion reinforces the conclusion that the circuit of Tosser's Fig. 6 is not a multiplexer (Br17). Dr. Sechen is a witness adverse to the patent owner in the related litigation (Br17). Figure 1 of Exhibit 14 of Dr. Sechen's deposition (Exhibit G to the brief) shows the same figure adapted from Tosser's Fig. 6 above. Dr. Sechen stated that "that circuit is certainly not a serial multiplexer." Deposition of Carl Sechen, Ph.D., August 18, 2003, at 161 (Exhibit G to brief). It is argued that "[m]ultiplexer circuits necessarily have terminals for control signals and distinct terminals for input variables" (Br17).

Patent owner's graphical arguments concerning Fig. 6 also apply to Fig. 9. We prefer to redraw Fig. 6 as shown below.



The structure of three multiplexers in series with three control variables (C1,C2,C3) and four input variables (I1,I2,I3,I4) is clearly present. Claim 47 reads on this structure (except for the TGMs) because it does not preclude the additional structure Tosser uses to implement the logic function, and because the actual inputs are not part of the claim. That is, claim 47 is directed to the bare multiplexer circuit, whereas Tosser shows the same multiplexer circuit (except for the TGMs) with the inputs connected to realize a specific logic function. The examples in Gorai also show serial multiplexer structures, as claimed (except for the TGMs), connected to realize specific logic functions.

(3)

It is argued that Gorai and Tosser do not teach that the input variables and control variables are independent of each other. It is argued that coupling an input terminal and a control terminal to receive the same variable, as in Fig. 9 of Tosser, which are coupled to receive $\overline{C}$ and C, respectively, is

"forbidden in a multiplexer circuit" (RBr12) and "[i]n the claimed multiplexer circuits, input variables are never applied to control input terminals, and control input signals are never applied to input terminals, and can never appear as outputs" (RBr12). Patent owner argues (RBr17) that the examiner errs in stating that "nowhere do the claims recite that the input variables are independent of each other, or that they are independent of the control inputs" (EA14-15). It is argued that the input variables are distinguished as first, second, third, and fourth input variables, the control signals are distinguished as first, second, and third control signals and "all variables have different names, indicating they are different" (RBr17).

As noted in the claim interpretation section, the variables are not part of the claims, which are directed to a multiplexer structure, not how it is used. Thus, it is sufficient that the input terminals are "capable of" being connected to independent control and input variables. Claim 47 does not require the first, second, third, and fourth input variables to be different variables from the control variables. It is not forbidden for a multiplexer to have some of the input variables set to be the same as some of the control variables. A multiplexer selects one of the input variables as an output. It makes no difference to the multiplexer structure whether the input variables are independent of each other or of the control variables, or whether the inputs are variables or constants; it is still a structure that selects one of the inputs to be output.

Nevertheless, Fig. 3 and the corresponding text of Gorai teaches that the input and control variables can all be independent. The structure of a 3-stage series of multiplexers can be connected to realize functions of seven or fewer variables without any change in the multiplexer structure itself.

Tosser shows a multiplexer structure as claimed (except for the use of TGMs) which is connected in certain ways to realize functions of four variables. The fact that the multiplexer is applied to realize functions of only four variables does not alter the fact that the structure could be connected to realize functions of seven variables.

(4)

It is argued that Gorai and Tosser teach combinational logic circuits, not multiplexer circuits. It is argued (RBr5) :

> Gorai teaches a specific way to cascade 2:1 multiplexer circuits to form combinational logic circuits in which inputs are combined to realize a logical function. In contrast, the pending claims are directed to multiplexer circuits in which one of a plurality of inputs is selected for delivery to an output, but in which no inputs are combined.

And (RBr9):

> Tosser, like Gorai, teaches a specific way to cascade multiplexer circuits to implement logic functions. In contrast, the pending claims are directed to multiplexer circuits in

> which one of a plurality of inputs is delivered to an output, not circuits that realize combinational logic.

Patent owner argues that the examiner errs in concluding (at EA16) that the combinational logic circuits of Gorai's Fig. 3 and Tosser's Fig. 9 are clearly performing a multiplexer function and in concluding that any circuit that includes a 2:1 multiplexer is a multiplexer regardless of the coupling of its inputs and outputs (RBr18). It is argued that under this interpretation, the buffer, NAND gate, and flip-flop illustrated in Exhibit D to the reply brief would become multiplexers, which is an unreasonable construction (RBr18). It is argued that a "multiplexer" is defined as "a hardware circuit for selecting a single output from multiple inputs," and that the circuits in Gorai and Tosser do not perform a multiplexer function (RBr18).

These arguments are totally without merit. Gorai teaches that "multiplexers (MUX) can be used as universal logic modules in the realisation of combinational circuits" (page 164). A multiplexer or a series of multiplexers can be utilized to implement combinational logic circuits, such as buffers and NAND circuits and more complicated functions, by selecting a single output from multiple inputs according to the control variables. For example, as noted in Appendix A, there are 16 logic functions of two variables that may be implemented with a 2:1 multiplexer (not all of which are useful), including AND, NAND, OR, and buffer functions. Multiplexers remain multiplexers no matter what logic circuit they implement by different connections of the

inputs. The claimed multiplexers will inherently realize combinational logic functions when they are connected to receive specific combinations of variables as patent owner is well aware. U.S. Patent 5,040,139 to Dzung J. Tran, the same inventor as the '666 patent, and also assigned to patent owner, shows the use of multiplexers to realize logic functions. And, if the discussions between TTI and Cadence involved the '666 patent's multiplexer, the primary use was to construct multi-level logic (Exhibit 4 to Tran declaration of Exhibit I).

(5)

It is argued that Gorai and Tosser teach using conventional binary tree multiplexers in their combinational logic circuits and do not suggest the claimed serial multiplexer circuits (Br19). It is argued that "[b]oth Tosser and Gorai turn to conventional [binary tree] multiplexer circuits whenever an N:1 multiplexer circuit is needed" (emphasis omitted) (Br19).

Apparently the argument is that Gorai and Tosser do not call a cascade arrangement of multiplexers a "multiplexer," so it must not be a multiplexer and the only multiplexers are the individual multiplexers that make up the network. Since Gorai and Tosser disclose a serial network of 2:1 multiplexers, the same structure as patent owner's invention, it is not known how patent owner can reasonably make this argument. The fact that a multiplexer structure can be connected in various ways to implement different logic functions does not mean that it is not a multiplexer.

(6)

It is argued that one skilled in the art would not arrive at the claimed 4:1 or 5:1 multiplexer circuits by following Gorai's synthesis method of generating a minterm table and applying an algorithm to the table. It is argued (RBr8-9):

> Because Gorai does not teach or suggest a minterm table for a serial multiplexer function, and provides no motivation to obtain such a minterm table or ratio parameters for a serial multiplexing function, Gorai necessarily fails to teach or suggest any such serial multiplexer circuits. Moreover, even if Gorai taught or suggested an appropriate minterm table, following Gorai's teaching of minterm table (ratio parameters) + algorithm = cascade circuit, would not produce the claimed multiplexer circuits. As stated in the Declaration of Joseph Tran (attached as Exhibit C [to the reply brief], submitted on September 17, 2003), following Gorai's procedure would produce a 4:1 multiplexer having six stages and a 5:1 multiplexer circuit having eight stages, not three or four stages recited in the pending claims. Therefore, using the method of Gorai to construct a multiplexer circuit having a truth table that is identical to that of the claimed 4:1 multiplexer circuits fails to produce the claimed multiplexer circuit.

The rejection does not rely on following Gorai's synthesis method. There is no need to follow Gorai's

synthesis method to realize a 4:1 or 5:1 multiplexer because Fig. 3 already shows a the p-stage serial multiplexer circuit which is a $(p+1)$:1 multiplexer.

(7)

Patent owner notes that the rejections of the 5:1 multiplexer claims appear to be based on a combination of Tosser modified to include an additional (fourth) stage and Weste (RBr19). It is argued that "even if Tosser disclosed 4:1 multiplexer circuits, Tosser expressly states that his method cannot be extended, and teaches away from providing a fourth stage such as recited in the 5:1 multiplexer circuit claims" (RBr19-20), so the "5:1 multiplexer circuit claims are separately patentable over the Tosser/Weste combination" (RBr20).

It is true that Tosser only expressly shows three multiplexer stages. Nevertheless, Tosser does not state that a cascade of multiplexers is limited to three stages; it only states that the synthesis method is limited to functions of six variables. The examiner concluded that one of ordinary skill in the art would have been motivated to extend the teaching of three stages of 2:1 multiplexers in Tosser to four stages to allow processing of more input signals (FR7) and patent owner has not shown any error in this reasoning. The rejection relies on the multiplexer structure shown in the figures, not on Tosser's method of synthesizing a logic circuit.

(8)

Patent owner argues that there is no motivation to combine the teachings of Gorai or

Tosser with Weste's TGM circuit (Br21-22). It is argued that Weste teaches that CMOS transistor pairs should be avoided in serial connections such as those recited in the pending claims because, "[a]ccording to Weste [at pages 174-175], pass transistor networks such as TGMs incur extra delays, exhibit higher internal node capacitances and higher series resistances, consume more circuit area, and require true and complement control variables" (Br22).

Weste discloses that pass transistor logic is popular in nMOS circuits and "the simplest example probably being a 2-input multiplexer" (page 172). Weste discloses (pages 174-175):

> The apparent advantages of pass transistor networks in CMOS should be studied carefully and judiciously utilized. A few points detract from the use of pass networks. To achieve good logic levels complementary pass networks are desirable but incur extra delay in pull-down. In comparison to regular gates, the merging of source and drain regions is difficult, leading to higher internal node capacitances. Finally true and complement control variables are required.

Thus, Weste disclose that pass transistor (transmission gate) networks have advantages and a few disadvantages. One skilled in the art would have been motivated to use TGMs for their known advantages and there is nothing that would lead one skilled in the art away from using TGMs.

Weste does not state that TGMs exhibit higher series resistances and consume more circuit area, as argued by patent owner. Patent owner is probably relying on the article by C. Zhang, Universal logic gate transmission gate array, Electronic Engineering, October 1985, pages 61-67, at page 63, which mentions these disadvantages for one circuit embodiment. Nevertheless, Zhang discloses that other circuits can overcome these problems. In any case, both Weste and Zhang disclose that TGMs are used for multiplexer circuits. Therefore, the advantages must outweigh whatever disadvantages TGMs might have, and one of ordinary skill in the art would not have been lead away from using TGMs; see EA21-22. Patent owner does not claim to have overcome the disadvantages of TGMs.

(9)

Patent owner argues that "[f]urther evidence of non-obviousness is set forth in a Statement Concerning Commercial Success and Other Objective Indicia of Non-Obviousness" (Br22).

This statement has been considered in the discussion of the objective evidence.

(10)

Patent owner argues that the examiner errs in stating (at EA14) that a variable and its logical complement, e.g., D and $\overline{D}$, are two different variables (RBr15-16).

We agree with patent owner that a variable and its logical complement are the same variable. A

variable and its complement represent different states of the same variable. However, the examiner's statement does not affect the decision. Gorai teaches that a *p*-stage serial arrangement of 2:1 multiplexers can receive *p* control variables and (*p*+1) input variables. The examples in Tosser and Gorai disclose a serial arrangement of three 2:1 multiplexers, which forms a multiplexer that meets the limitations of claim 47 (except for the TGMs). The fact that the examples show the multiplexer arrangement connected in specific ways to realize specific functions of less than the number of variables that could be handled is not important because: (1) the claims are open ended and do not preclude the additional structure that is used to connect the input terminals of the multiplexers to specific variables; and (2) the input variables are not part of the claimed structure. Since the multiplexer structure is disclosed in the examples, patent owner can at most argue that connecting different inputs to the multiplexer than the ones shown in the examples is a new use of an old machine. However, the use is not new since the multiplexers are intended to multiplex any set of inputs and, furthermore, the input signal variables are not part of the claimed structure. Also, a new use would have to be claimed as a process claim. 35 U.S.C. § 100(b).

(11)

Patent owner argues that the examiner errs in stating (at EA15-16) that input signals are all "input variables" regardless of whether or not they are set to a constant value because a constant (0 or 1) is not a variable (RBr16-17).

We agree that a constant (0 or 1) is not a variable. A variable must be capable of assuming, at any given time, either one of at least two values (0 or 1), whereas a constant has a fixed value. Gorai distinguishes between variables and constants; e.g., "the remaining 8 variables, or their complements or constant (0 or 1)" (page 164) and "[f]or the last stage g_p is reduced to a single variable or constant 0 or 1" (page 166). However, since the input signals are not part of the claimed structure, it does not matter whether the inputs are variables or constant as long as the multiplexer is capable of handling variables.

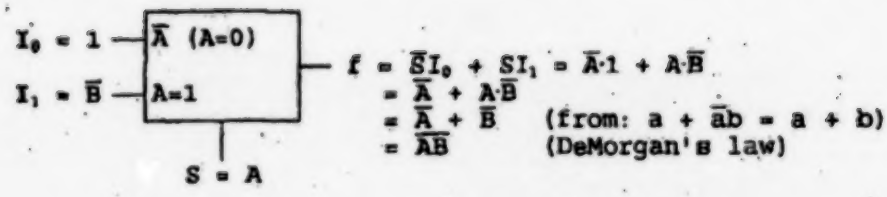
It is argued (RBr17):

> When the input of a TG [transmission gate) is coupled to receive a variable, the TG functions as a multiplexer. When the input of a TG is coupled to receive a constant, the TG functions as a logic gate such as a NAND, NOR, or buffer. Representative logic gates coupled in this manner are shown in Exhibit D. If a constant were a variable, then the buffer circuit shown in Exhibit D would be a multiplexer. It is not.

This argument is incorrect. A multiplexer selects one of the input variables as an output and has the truth table shown in Table 1.4 (page 17) of Weste and in Exhibit D to the reply brief (where each "X" in Table 1.4 of West is a "don't care" that can be replaced by either a "0" or a "1" to give the truth table of Exhibit D). The multiplexer structure is the same whether the data inputs are variables or constants. The only difference is that there are

fewer rows in the truth table when one or both inputs are a constant. Gorai discusses that the control inputs to a multiplexer are variables, while the data inputs can be a variable, its complement, or a constant (0 or 1) (page 165). As apparent from the example for an *M(3)* in Gorai (page 165), for a 2:1 multiplexer *M(1)*, there are two variables, two complements, and a constant (0 or 1) (6 possible input values) that can be applied to each input , for a total of 6^2 distinct-functions that can be realized. when the inputs are limited to variables, only 4^2 functions can be realized. In any case, the multiplexer performs as a multiplexer whether the inputs are constant, variables, or a mix of constants and variables.

The buffer in Exhibit D to the reply brief is a multiplexer with one input connected to the supply voltage V (a logical "1") and the other input connected to ground (a logical "0"). When the control variable A=1, the multiplexer selects the supply voltage V, and when A=0 ($\overline{A}$=1), the multiplexer selects ground. Similarly, the multiplexer for the NAND gate selects between a constant supply voltage V (a logical "1") and a variable complement $\overline{B}$. The multiplexer acts as a multiplexer regardless of whether the inputs are constants or variables. While patent owner has drawn the logic symbols, functions, and truth tables in Exhibit D to appear as different as possible from the those for the multiplexer, each logic function is, in fact, one connection of the multiplexer. For example, NAND gate can be drawn using the multiplexer symbol and function in Exhibit D:



The multiplexer selects a "1" if A=0 and selects "$\overline{B}$" if A=1. The truth table with entries for all the inputs is

S=A	$I_1=\overline{B}$	$I_0=1$	F
0	0	1	1
0	1	1	1
1	0	1	0
1	1	1	1

This can be redrawn as a function of A and B as in Exhibit D. The truth table contains half the number of rows as the general multiplexer truth table because input I_0 is a constant.

(12)

Patent owner argues that the examiner errs in finding (at EA15) that the internal outputs of the first and second multiplexer stages in Fig. 3 of Gorai are "input signals" (RBr17-18). It is argued that the examiner's interpretation of these internal signals as "input signals" is not reasonable because it strips the word "input" of meaning (RBr18).

The claims recite "input variables," not "input signals." We agree with patent owner that the outputs of the multiplexers can not be construed as the claimed "input variables." The claims recite that the TGM circuit signal input terminal not coupled to a previous stage output terminal is "coupled to receive" the "input variable"; thus, the TGM output cannot be an "input variable." However, the examiner points out that Fig. 3 of Gorai (for $p = 3$) shows seven input variables besides the two internal inputs from the multiplexers (EA15). Accordingly, it is not necessary to rely on the TGM outputs as "input variables" and the examiner's statement is harmless.

(13)

It is noted (RBr19) that the examiner's answer finds that "both Tosser and Gorai clearly teach 4:1 multiplexer circuits having three cascaded stages, and lack only the teaching to implement the stages using the well-known transmission gate multiplexer [TGM] circuits" (EA8). It is argued that "[i]f the Answer contends that, absent the recited TGM circuits, the rejections are based on some other modifications of either Tosser or Gorai, or require features not found in either Tosser or Gorai, Patentee requests clarification and an opportunity to respond to such a rejection" (RBr19).

Patent owner correctly understands that the examiner finds the only difference between the claimed 4:1 multiplexer in claim 47 and the p-stage (with p=3) multiplexer in Gorai's Fig. 3 and the 3-stage multiplexer in Tosser is the use of TGMs. The examiner finds that the claimed 5:1 multiplexer with

4 stages in claim 48 is disclosed by the *p*-stage (with *p*=4) multiplexer in Gorai's Fig. 3 except for the TGMs. The examiner recognizes that a 4-stage serial multiplexer and the use of TGMs is not shown in Tosser, but concludes that one skilled in the art would have been motivated to modify the 3-stage multiplexer in Tosser to add an additional stage to allow processing of more input signals (FR7). This opinion does not alter the examiner's rejection.

(14)

Patent owner argues that the examiner incorrectly concluded that the licensing discussed in Mr. Tran's declaration under 37 C.F.R. § 1.132 concerning commercial success is mere potential licensing, whereas the declaration and accompanying exhibits demonstrate actual, not potential licensing (RBr19).

The only actual licensing is the licensing to Intel Corp. As discussed in the analysis of the objective evidence, it is not known exactly what was licensed and patent owner has established no nexus between what was licensed and the claims of the '666 patent. The other evidence about discussions with Cadence, National Semiconductor, and Hewlett-Packard show only that these companies might be interested in something (not identified) by TTI, not that any licensing took place. We further agree with the examiner's appraisal that this evidence does not rise to the level of actual "licensing" or "commercial success" (EA23).

CONCLUSION

The rejections of claims 16, 17, 39-45, 47, and 48 are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136 (a). See 37 C.F.R. § 1.136 (a) (1) (iv).

AFFIRMED

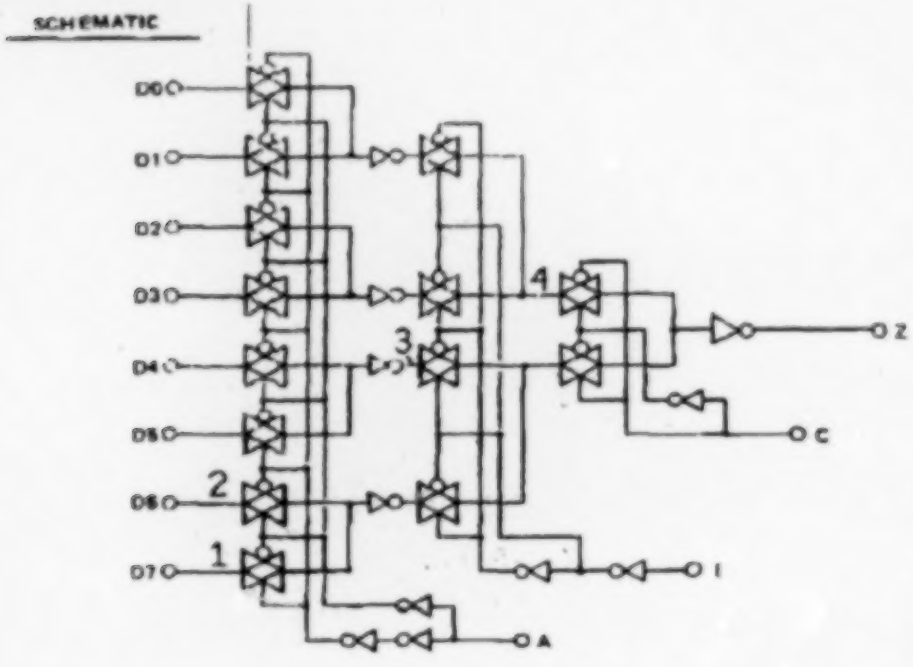
s/Errol A. Krass	)	
ERROL A. KRASS	)	
Administrative Patent Judge	)	BOARD OF PATENT
	)	APPEALS AND
	)	INTERFERENCES
s/Robert Nappi	)	
ROBERT NAPPI	)	
Administrative Patent Judge	)	

BARRETT, Administrative Patent Judge.

These additional comments are added because I think it should be pointed out that claim 47 is anticipated by the Toshiba TC19G000 Series, MUX8 Macrocell Data Sheet, page 1-110, May 1986, reproduced in Appendix D, and that claim 48 would have been obvious over Toshiba MUX8 in view of patent owner's admissions. I write separately because the panel does not want to raise any question of a new ground of rejection in the main opinion.

The Toshiba MUX8 reference was cited by the inventor in the background of the '666 patent (col. 1, lines 31-34). The Toshiba MUX8 multiplexer is a binary tree arrangement of 2:1 transmission gate multiplexers (TGMs) having four TGMs in the first stage controlled by control input A, two TGMs in the second stage controlled by control input B, and one TGM in the third stage controlled by control input C, forming an 8:1 multiplexer.

Claim 47 is an open-ended claim and does not preclude additional structure. It can be easily seen that the Toshiba MUX8 anticipates the subject matter of claim 47 from the figure on the next page in which the structure of claim 47 is shown in black lines (having four data input variables 1, 2, 3, and 4, and three control variables A, B, and C) and the additional structure not precluded by claim 47 is shown in gray.



The instant reexaminations were all filed before the changes to 35 U.S.C. §§ 303(a) and 312(a) allowing consideration of old art in a reexamination proceeding. See In re Bass, 314 F.3d 575, 576 n.*, 65 USPQ2d 1156, 1157 n.* (Fed. Cir. 2002). Although we do not find any reference to the Toshiba MUX8 reference in the reexaminations, this may be because it was thought not to be permitted. This case is a good example of why old art, which may not have been fully appreciated by the examiner, should be allowed to be considered in a reexamination.

The '666 patent admits that known multiplexer circuits are built up of a binary tree arrangement of 2-input multiplexers and can have any number N input variables (col. 1, lines 9-39). In particular, there can be 16 multiplexer circuits in the first stage (col. 1, line 38), requiring four stages. It would have been obvious to one of ordinary skill in the art to extend the 8:1 binary tree arrangement of TGMs as taught by Toshiba MUX8 to a known 16:1 multiplexer in view of patentee's admission and such a four stage arrangement of 2:1 multiplexers contains the 5:1 multiplexer of claim 48.

s/Lee E. Barrett
LEE E. BARRETT
Administrative Patent Judge

) BOARD OF PATENT
) APPEALS AND
) INTERFERENCES

KLARQUIST SPARKMAN, LLP 121 SW SALMON STREET SUITE 1600 PORTLAND, OR 97204	Attorney for Patent Owner
ALAN R. LOUDERMILK LOUDERMILK & ASSOCIATES P.O. BOX 3607 LOS ALTOS, CA 94024-0607	Third Party Requester

APPENDIX N

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

2005-1387, 2006-1333

TRANSLOGIC TECHNOLOGY, INC.,

Plaintiff-Appellee,

v.

HITACHI, LTD., HITACHI AMERICA, LTD. AND RENESAS TECHNOLOGY AMERICA, INC.,

Defendants-Appellants.

Appeal from the United States District Court for the District of Oregon in case no. CV 99-407, Senior Judge Owen M. Panner.

ORDER

NOTE: This order is nonprecedential.

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

ORDER

A combined petition for panel rehearing and for rehearing en banc having been filed by the Appellee, and a response thereto having been invited by the court and filed by the Appellants, and the petition for rehearing and response, having been referred to the panel that heard the appeal, and thereafter the petition for rehearing en banc and response having been referred to the circuit judges who are in regular active service,

UPON CONSIDERATION THEREOF, it is

ORDERED that the petition for panel rehearing be, and the same hereby is, DENIED and it is further

ORDERED that the petition for rehearing en banc be, and the same hereby is, DENIED.

The mandate of the court will issue on June 5, 2008.

FOR THE COURT,

/s/ Jan Horbaly/JB
Jan Horbaly
Clerk

Dated: 05/29/2008

cc: James G. Gilliland, Jr.
Richard L. Rainey

FILED

U.S. COURT OF
APPEALS FOR THE
FEDERAL CIRCUIT

MAY 29 2008

JAN HORBALY
Clerk

TRANSLOGIC TECH V HITACHI LTD, 2005-1387, 2006-1333 (DCT - CV 99-407)